Hitachi Global Storage Technologies

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Hard Disk Drive Specification

Hitachi Deskstar P7K500

Hitachi CinemaStar P7K500

3.5 inch hard disk drive

Models:

HDP725016GLAT80	HCP725016GLAT80
HDP725016GLA380	HCP725016GLA380
HDP725025GLAT80	HCP725025GLAT80
HDP725025GLA380/1	HCP725025GLA380
HDP725032GLAT80	HCP725032GLAT80
HDP725032GLA380	HCP725032GLA380
HDP725032GLA360/1	HCP725050GLAT80
HDP725040GLAT80	HCP725050GLA380
HDP725040GLA380	
HDP725040GLA360/1	
HDP725050GLAT80	
HDP725050GLA380	
HDP725050GLA360/1	

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1.0 General

1.1 Introduction

This document describes the specifications of the Deskstar P7K500 and Cinemastar P7K500, an Hitachi Global Storage Technologies 3.5-inch 7200-rpm ATA interface hard disk drive with the following model numbers:

- Deskstar models
  - HDP725016GLAT80 / A380 (160.0 GB)
  - HDP725025GLAT80 / A380 / A381 (250.0 GB)
  - HDP725032GLAT80 / A380 / A360 / A361 (320.0 GB)
  - HDP725040GLAT80 / A380 / A360 / A361 (400.0 GB)
  - HDP725050GLAT80 / A380 / A360 / A361 (500.0 GB)
- Cinemastar models
  - HCP725016GLAT80 / A380 (160.0 GB)
  - HCP725025GLAT80 / A380 (250.0 GB)
  - HCP725032GLAT80 / A380 (320.0 GB)
  - HCP725050GLAT80 / A380 (500.0 GB)

Part 1 defines the functional specification.

1.2 Glossary

ESD	Electrostatic Discharge
Kbpi	1,000 bits per inch
Ktpi	1,000 tracks per inch
Mbps	1,000,000 bits per second
GB	1,000,000,000 bytes
MB	1,000,000 bytes
KB	1,000 bytes unless otherwise specified
32KB	32 x 1024 bytes
64KB	64 x 1024 bytes
S.M.A.R.T.	Self-Monitoring Analysis and Reporting Technology
DFT	Drive Fitness Test
ADM	Automatic Drive Maintenance

1.3 Caution

The drive can be damaged by shock or ESD (Electrostatic Discharge). Any damage sustained by the drive after removal from the shipping package and opening the ESD protective bag are the responsibility of the user.

1.4 References

- Information Technology-AT Attachment with Packet Interface-8
- Serial ATA II: Extensions to Serial ATA 1.0
- Serial ATA International Organization: Serial ATA Revision 2.60

2.0 General features

- Data capacities of 160B - 500GB
- Spindle speeds of 7200 RPM
- Fluid Dynamic Bearing motor
- Enhanced IDE interface / Serial ATA interface
- Sector format of 512 bytes/sector
- Closed-loop actuator servo
- Load/Unload mechanism, non head disk contact start/stop
- Automatic Actuator lock
- Interleave factor 1:1
- Seek time of 14 ms(1D/2D) typical without Command Overhead
- Sector Buffer size of 8192 KB(1D/2D) / 16384 KB(2D) (Upper 1000 KB / 1248.KB is used for firmware)
- Ring buffer implementation
- Write Cache
- Native command queuing support (SATA model)
- Advanced ECC On The Fly (EOF)
- Automatic Error Recovery procedures for read and write commands
- Self Diagnostics on Power on and resident diagnostics
- Parallel ATA PIO Register/Data Transfer Mode 4 (16.6 MB/sec)
- Parallel ATA DMA Data Transfer
  - Multiword mode Mode 2 (16.6 MB/sec)
  - Ultra DMA Mode 6 (133 MB/sec)
- Serial ATA Data Transfer 3Gbps/1.5Gbps
- CHS and LBA mode
- Power saving modes/Low RPM idle mode (APM)
- S.M.A.R.T. (Self Monitoring and Analysis Reporting Technology)
- Support security feature
- Quiet Seek mode (AAM)
- 48 bit addressing feature
- ATA-8 compliant
  - UDMA133 support
  - Streaming feature set support
  - World Wide Name
  - Write Uncorrectable
- SATA 2.6 compliant

Part 1. Functional specification

3.0 Fixed disk subsystem description

3.1 Control Electronics

The drive is electronically controlled by a microprocessor, several logic modules, digital/analog modules, and various drivers and receivers. The control electronics performs the following major functions:

- Controls and interprets all interface signals between the host controller and the drive.
- Controls read write accessing of the disk media, including defect management and error recovery.
- Controls starting, stopping, and monitoring of the spindle.
- Conducts a power-up sequence and calibrates the servo.
- Analyzes servo signals to provide closed loop control. These include position error signal and estimated velocity.
- Monitors the actuator position and determines the target track for a seek operation.
- Controls the voice coil motor driver to align the actuator in a desired position.
- Constantly monitors error conditions of the servo and takes corresponding action if an error occurs.
- Monitors various timers such as head settle and servo failure.
- Performs self-checkout (diagnostics).

3.2 Head disk assembly

The head disk assembly (HDA) is assembled in a clean room environment and contains the disks and actuator assembly. Air is constantly circulated and filtered when the drive is operational. Venting of the HDA is accomplished via a breather filter.

The spindle is driven directly by an in-hub, brushless, sensorless DC drive motor. Dynamic braking is used to quickly stop the spindle.

3.3 Actuator

The read/write heads are mounted in the actuator. The actuator is a swing-arm assembly driven by a voice coil motor. A closed-loop positioning servo controls the movement of the actuator. An embedded servo pattern supplies feedback to the positioning servo to keep the read/write heads centered over the desired track.

The actuator assembly is balanced to allow vertical or horizontal mounting without adjustment.

When the drive is powered off, the actuator automatically moves the head to the actuator ramp outside of the disk where it parks.

4.0 Drive characteristics

This section describes the characteristics of the drive.

4.1 Default logical drive parameters

The default of the logical drive parameters in Identify Device data is as shown below.

Description	HDP725016GLxxxx HCP725016GLxxxx	HDP725025GLxxxx HCP725025GLxxxx
Physical Layout		
Label capacity (GB)	160	250
Bytes per Sector	512	512
Number of Heads	2	2
Number of Disks	1	1
Logical Layout[2]		
Number of Heads	16	16
Number of Sectors/ Track	63	63
Number of Cylinders[1]	16,383	16,383
Number of Sectors	312,581,808	488,397,168
Total Logical Data Bytes	160,041,885,696	250,059,350,016
Description	**HDP725032GLxxxx**[2] **HCP725032GLxxxx**	
Physical Layout		
Label capacity (GB)	320	
Bytes per Sector	512	
Number of Heads	3	
Number of Disks	2	
Logical Layout[2]		
Number of Heads	16	
Number of Sectors/ Track	63	
Number of Cylinders[1]	16,383	
Number of Sectors	625,142,448	
Total Logical Data Bytes	320,072,933,376	
Description	**HDP725040GLxxxx**[3] **HCP725040GLxxxx**	**HDP725050GLxxxx**[3] **HCP725050GLxxxx**
Physical Layout		
Label capacity (GB)	400	500
Bytes per Sector	512	512
Number of Heads	4	4
Number of Disks	2	2
Logical Layout[2]		
Number of Heads	16	16
Number of Sectors/ Track	63	63
Number of Cylinders[1]	16,383	16,383
Number of Sectors	781,422,768	976,773,168
Total Logical Data Bytes	400,088,457,216	500,107,862,016

Table 1 Formatted capacity

Notes: [1] Number of cylinders: For drives with capacities greater an 8.45 GB the IDENTIFY DEVICE information word 01 limits the number of cylinders to 16,383 per the ATA specification.

[2] Logical layout: Logical layout is an imaginary drive parameter (that is, the number of heads) which is used to access the drive from the system interface. The Logical layout to Physical layout (that is, the actual Head and Sectors) translation is done automatically in the drive. The default setting can be obtained by issuing an IDENTIFY DEVICE command

[3] HDP7250xxVLA381/361 is iVDR model.

4.2 Data sheet

Description	160 Model	250GB Model	320GB Model	400GB Model	500GB Model
Data transfer rate (Mbps)	1075	1138	1075	1075	1138
Interface transfer rate (MB/s)	133(PATA) / 300(SATA)				
Data buffer size[1] (KB)	8,192/16384				
Rotational speed (RPM)	7,200				
Number of buffer segments (read)	up to 128				
Number of buffer segments (write)	up to 63				
Recording density- max (Kbpi)	970	1097	989	970	1097
Track density (Ktpi)	160	168	164	160	168
Areal density - max (Gbits/in^2)	155	185	162	155	185
Number of data bands	31				

[1]Upper 1000 KB / 1248 KB is used for firmware

Table 2 Mechanical positioning performance

4.3 World Wide Name Assignment

Description of	160GB Model	250GB Model	320GB Model	400GB Model	500GB Model
Organization	Hitachi GST				
Manufacturing Site	HGST China Plant, China(GSP) ExcelStor Plant, China(EST)		HGST China Plant, China(GSP)		
Product	Gemini - Deskstar P7K750 / CinemaStar P7K750				
OUI	000CCAh				
SHBU Block Assignment	32Ah(GSP) 329h(EST)		32Bh(GSP)	32Ch(GSP)	
Port/Node ID	11b				

Table 3 World Wide Name Assignment

4.4 Drive organization

4.4.1 Drive format

Upon shipment from Hitachi Global Storage Technologies manufacturing the drive satisfies the sector continuity in the physical format by means of the defect flagging strategy described in Section 5.0 on page 14 in order to provide the maximum performance to users.

4.4.2 Cylinder allocation

Physical cylinder is calculated from the starting data track of 0. It is not relevant to logical CHS. Depending on the capacity some of the inner zone cylinders are not allocated.

Data cylinder
This cylinder contains the user data which can be sent and retrieved via read/write commands and a spare area for reassigned data.

Spare cylinder
The spare cylinder is used by Hitachi Global Storage Technologies manufacturing and includes data sent from a defect location.

4.5 Performance characteristics

Drive performance is characterized by the following parameters:

- Command overhead
- Mechanical positioning
  - Seek time
  - Latency
- Data transfer speed
- Buffering operation (Look ahead/Write cache)

All the above parameters contribute to drive performance. There are other parameters that contribute to the performance of the actual system. This specification defines the characteristics of the drive, not the characteristics of the system throughput which depends on the system and the application.

4.5.1 Command overhead

Command overhead is defined as the time required

- from the time the command is written into the command register by a host
- to the assertion of DRQ for the first data byte of a READ command when the requested data is not in the buffer
- excluding Physical seek time and Latency

The table below gives average command overhead.

Command type (Drive is in quiescent state)	**Time (Typical) (ms)**	**Time (Typical) for NCQ command (ms)***
Read (Cache not hit) (from Command Write to Seek Start)	0.5	0.5
Read (Cache hit) (from Command Write to DRQ)	0.1	0.2
Write (from Command Write to DRQ)	0.015	0.2
Seek (from Command Write to Seek Start)	0.5	not applicable

* SATA only

Table 4 Command overhead

4.5.2 Mechanical positioning

4.5.2.1 Average seek time (without command overhead, including settling)

Command Type	1D/2D	
	Typical (ms)	**Max** (ms)
Read	14.0	14.7
Write	15.0	15.7

Table 5 Mechanical positioning performance

The terms “Typical” and “Max” are used throughout this specification with the following meanings:

Typical. The average of the drive population tested at nominal environmental and voltage conditions.

Max. The maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See Section 6.4, “Environment” on page 41 and Section 6.5, “DC Power Requirements” on page 43.

Seek time is measured from the start of the motion of the actuator to the start of *a reliable read or write operation.* "Reliable read or write" implies that error correction/recovery is not used to correct arrival problems. The average seek time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{\text{max.}} (\text{max.} + 1 - n)\,(Tn_{in} + Tn_{out})}{(\text{max.} + 1)\,(Tn_{in} + Tn_{out})}$$

where: max = maximum seek length
n = seek length (1 to max)
Tn_{in} = inward measured seek time for an n-track seek
Tn_{out} = outward measured seek time for an n-track seek

4.5.2.2 Full stroke seek (without command overhead, including settling)

Command Type	1D/2D	
	Typical (ms)	**Max** (ms)
Read	27.0	30.0
Write	28.0	31.0

Table 6 Full stroke seek time

Full stroke seek is measured as the average of 1000 full stroke seeks with a *random head switch* from both directions (inward and outward).

4.5.2.3 Single track seek time (without command overhead, including settling)

Common to all models and all seek modes

Function	Typical (ms)	Max (ms)
Read	0.8	1.5
Write	1.3	2.0

Table 7 Single Track Seek Time

Single track seek is measured as the average of one (1) single track seek from every track with a random head switch in both directions (inward and outward).

4.5.2.4 Average latency

Rotational speed	Time for a revolution (ms)	Average latency (ms)
7200 RPM	8.3	4.17

Table 8 Latency Time

4.5.3 Drive ready time

Power on to ready	**Typical** (sec)	**Maximum** (sec)
1D model	8	20
2D model	10	20

Table 9 Drive ready time

Ready The condition in which the drive is able to perform a media access command (such as read, write) immediately.

Power on This includes the time required for the internal self diagnostics.

Note: Max Power On to ready time is the maximum time period that Device 0 waits for Device 1 to assert PDIAG–.

4.5.4 Operating modes

4.5.4.1 Operating mode descriptions

Operating mode	Description
Spin-up	Start up time period from spindle stop or power down
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Unload Idle	Spindle rotation at 7200 RPM with heads unloaded
Idle	Spindle motor and servo system are working normally. Commands can be received and processed immediately
Standby	Actuator is unloaded and spindle motor is stopped. Commands can be received immediately
Sleep	Actuator is unloaded and spindle motor is stopped. Only soft reset or hard reset can change the mode to standby

Note: Upon power down or spindle stop a head locking mechanism will secure the heads in the OD parking position.

4.5.4.2 Mode transition times

Mode transition times are shown below.

From	To	RPM	Transition time (typical) (sec)	Transition time (max) (sec)
Standby	Idle	0 -> 7200	8(1D)/10(2D)	20
Idle	Standby	7200 -> 0	Immediately	Immediately
Standby	Sleep	0	Immediately	Immediately
Sleep	Standby	0	Immediately	Immediately
Unload Idle	Idle	7,200	0.7	1
Idle	Unload Idle	7,200	0.7	1
Low RPM Idle	Idle	4500 -> 7200	3(1D)/4(2D)	10

Note: The command is processed immediately but there will be an actual spin down time reflecting the seconds passed until the spindle motor stops.

Table 10 Mode transition times

5.0 Defect flagging strategy

Media defects are remapped to the next available sector during the Format Process in manufacturing. The mapping from LBA to the physical locations is calculated by an internally maintained table.

Shipped format

- Data areas are optimally used.
- No extra sector is wasted as a spare throughout user data areas.
- All pushes generated by defects are absorbed by the spare tracks of the inner zone.

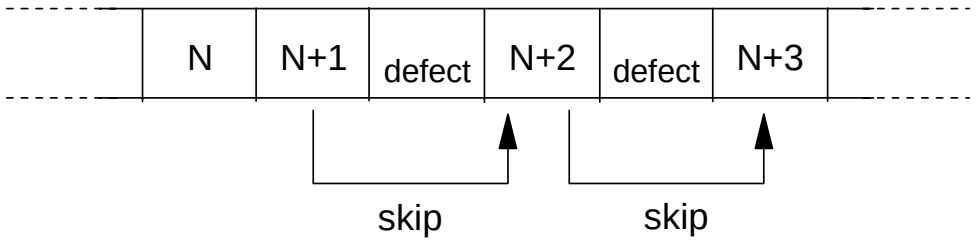


Figure 1 PList physical format

Defects are skipped without any constraint, such as track or cylinder boundary. The calculation from LBA to physical is done automatically by internal table. Specification

5.1 Electrical interface

5.1.1 Connector location

Refer to the following illustration to see the location of the connectors.

PATA MODEL

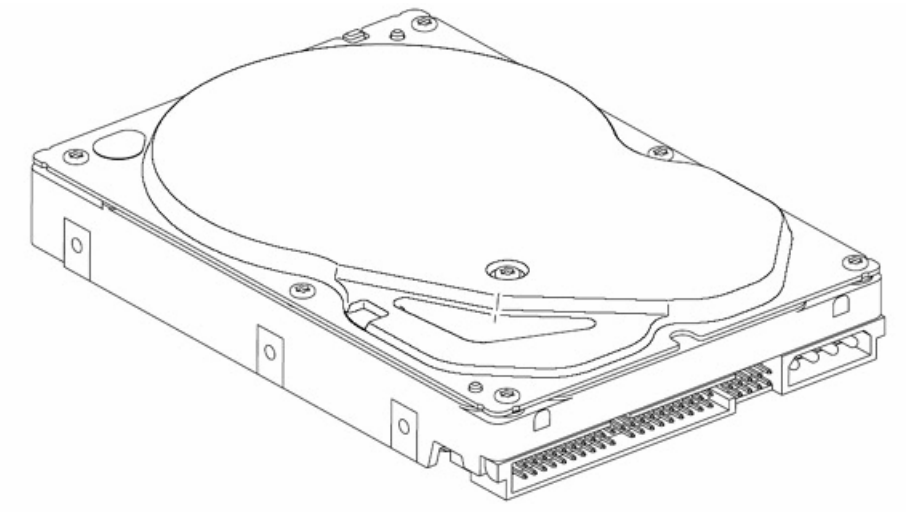


Figure 2 Connector location (PATA)

SATA MODEL

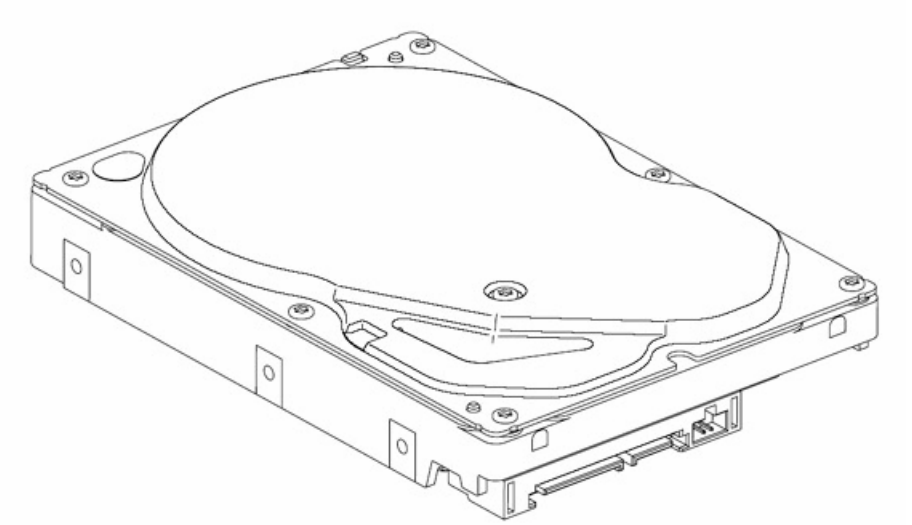
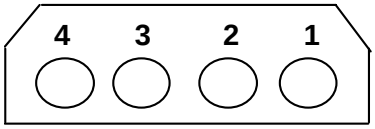


Figure 3 Connector location (SATA)

5.1.1.1 4pin DC power connector (only for PATA)

The DC power connector is designed to mate with AMP part number 1-480424-0 using AMP pins part number 350078-4 (strip), part number 61173-4 (loose piece), or their equivalents. Pin assignments are shown in the figure below.



Pin	Voltage
1	+12 V
2	GND
3	GND
4	+5V

Figure 4 Power connector pin assignments

5.1.1.2 signal connector

The AT signal connector is a 40-pin connector.

The SATA signal connector is a 8-pin connector. Power connector is a 15-pin connector. (SATA Model)

5.1.2 Signal definition(PATA model)

The pin assignments of interface signals are listed in the figure below:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	RESET-	I	TTL	02	GND		
03	DD7	I/O	3-state	04	DD8	I/O	3-state
05	DD6	I/O	3-state	06	DD9	I/O	3-state
07	DD5	I/O	3-state	08	DD10	I/O	3-state
09	DD4	I/O	3-state	10	DD11	I/O	3-state
11	DD3	I/O	3-state	12	DD12	I/O	3-state
13	DD2	I/O	3-state	14	DD13	I/O	3-state
15	DD1	I/O	3-state	16	DD14	I/O	3-state
17	DD0	I/O	3-state	18	DD15	I/O	3-state
19	GND			(20)	key		
21	DMARQ	O	3-state	22	GND		
23	DIOW-(*)	I	TTL	24	GND		
25	DIOR-(*)	I	TTL	26	GND		
27	IORDY(*)	O	3-state	28	CSEL	I	TTL
29	DMACK-	I	TTL	30	GND		
31	INTRQ	O	3-state	32	I		
33	DA1	I	TTL	34	PDIAG-	I/O	OC
35	DA0	I	TTL	36	DA2	I	TTL
37	CSO-	I	TTL	38	CS1-	I	TTL
39	DASP-	I/O	OC	40	GND		

Table 11 Table of signals

Notes:

1. "O" designates an output from the drive.
2. "I" designates an input to the drive.
3. "I/O" designates an input/output common.
4. "OC" designates open-collector or open-drain output.
5. The signal lines marked with (*) are redefined during the Ultra DMA protocol to provide special functions. These lines change from the conventional to special definitions at the moment the Host decides to allow a DMA burst if the Ultra DMA transfer mode was previously chosen via SetFeatures. The Drive becomes aware of this change upon assertion of the DMACK- line. These lines revert back to their original definitions upon the deassertion of DMACK- at the termination of the DMA burst.

	Special Definition (for Ultra DMA)	Conventional Definition
Write Operation	DDMARDY- HSTROBE STOP	IORDY DIOR- DIOW-
Read Operation	HDMARDY- DSTROBE STOP	DIOR- IORDY DIOW-

Table 12 Signal special definitions for Ultra DMA

DD0-DD15 16-bit bi-directional data bus between the host and the drive. The lower 8 lines, DD00-07, are used for Register and ECC access. All 16 lines, DD00-15, are used for data transfer. These are 3-State lines with 24 mA current sink capability.

DA0-DA2 Address used to select the individual register in the drive.

CS0- Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error {Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status {Command when written} register) can be selected. (See Table 26: "I/O address map" on page 34)

CS1- Chip select signal generated from the Host address bus. When active one of the Control Block Registers (Alternate Status {Device Control when written}) can be selected. (See Table 26: "I/O address map" on page 34)

RESET- This line is used to reset the drive. It shall be kept in Low logic state during power up and in High thereafter.

DIOW- Its rising edge holds data from the host data bus to a register or data register of the drive.

DIOR- When low, this signal enables data from a register or data register of the drive onto data bus. The data on the bus shall be latched on the rising edge of DIOR-.

INTRQ Interrupt is enabled only when the drive is selected and the host activates the nIEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 24 mA sink capability.

DASP- This is a time-multiplexed signal which indicates that a drive is active, or that device 1 is present. This signal is driven by Open-Drain driver and internally pulled up to 5 volts through a 10kΩ resistor.

During Power-On initialization or after RESET- is negated, DASP- shall be asserted by Device 1 within 400 ms to indicate that device 1 is present. Device 0 shall allow up to 450 ms for device 1 to assert DASP-. If device 1 is not present, device 0 may assert DASP- to drive a LED indicator.

DASP- shall be negated following acceptance of the first valid command by device 1. At anytime after negation of DASP-, either drive may assert DASP- to indicate that a drive is active.

PDIAG- PDIAG- shall be asserted by device 1 to indicate to device 0 that it has completed diagnostics. This line is pulled-up to 5 volts in the drive through a 10kΩ resistor.

Following a Power On Reset, software reset, or RESET-, drive 1 shall negate PDIAG- within 1 ms (to indicate to device 0 that it is busy). Drive 1 shall then assert PDIAG- within 30 seconds to indicate that it is no longer busy and is able to provide status.

Following the receipt of a valid Execute Drive Diagnostics command, device 1 shall negate PDIAG- within 1 ms to indicate to device 0 that it is busy and has not yet passed its drive diagnostics. If device 1 is present, device 0 shall wait up to 6 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert PDIAG-. Device 1 should clear BSY before asserting PDIAG-, as PDIAG- is used to indicate that device 1 has passed its diagnostics and is ready to post status.

If device 1 did not assert DASP- during reset initialization, device 0 shall post its own status immediately after it completes diagnostics and clear the device 1 Status register to 00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

Device 1 shall release PDIAG-/CBLID- no later than after the first command following a power on or hardware reset sequence so that the host may sample PDIAG-/CBLID- in order to detect the presence or absence of an 80-conductor cable assembly.

CSEL (Cable Select) (Optional)

The drive is configured as either Device 0 or 1 depending upon the value of CSEL.

- If CSEL is grounded, the device address is 0.
- If CSEL is open, the device address is 1.

KEY Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion by mistake.

IORDY This signal is negated to extend the host transfer cycle when a drive is not ready to respond to a data transfer request and may be negated when the host transfer cycle is less than 240 ns for PIO data transfer. This signal is an open-drain output with 24 mA sink capability and an external resistor is needed to pull up this line to 5 volts.

DMACK- This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted or that data is available.

This signal is internally pulled up to 3.3 V through a 15 KΩ resistor. The tolerance of the resistor value is –50% to +100%.

DMARQ This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used on a handshake manner with DMACK-. This signal is a 3-state line with 24mA sink capability and internally pulled down to GND through 10 KΩ resistor.

HDMARDY- (Ultra DMA)

This signal is used only for Ultra DMA data transfers between the host and the device.

HDMARDY- is a flow control signal for Ultra DMA data in bursts. This signal is held asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data in transfers. The host may negate HDMARDY- to pause an Ultra DMA data in transfer.

HSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between the host and the device.

HSTROBE is the data out strobe signal from the host for an Ultra DMA data out transfer. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop toggling HSTROBE to pause an Ultra DMA data out transfer.

STOP (Ultra DMA)

This signal is used only for Ultra DMA data transfers between the host and the device.

STOP shall be asserted by the host prior to initiation of an Ultra DMA burst. STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during or after data transfer in an Ultra DMA mode signals the termination of the burst.

DDMARDY- (Ultra DMA)

This signal is used only for Ultra DMA data transfers between the host and the device.

DDMARDY- is a flow control signal for Ultra DMA data out bursts. This signal is held asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out transfers. The device may negate DDMARDY- to pause an Ultra DMA data out transfer.

DSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between the host and the device.

DSTROBE is the data in strobe signal from the device for an Ultra DMA data in transfer. Both the rising and falling edge of DSTROBE latch the data from DD(15:0) into the host. The device may stop toggling DSTROBE to pause an Ultra DMA data in transfer.

Device Termination

The termination resistors on the device side are implemented on the drive side as follows:

- 33 Ω for DD0 thru DD15, DMARQ, INTRQ
- 82 Ω for CS0-, CS1-, DA0, DA1, DA2, DIOR-, DIOW-, DMACK-
- 22 Ω for IORDY

5.1.3 Interface logic signal levels(PATA model)

The interface logic signal has the following electrical specifications:

Inputs	Input High Voltage	2.0 V min.
	Input Low Voltage	0.8 V max.
Outputs	Output High Voltage	2.4 V min.
	Output Low Voltage	0.5 V max.

5.1.4 Signal definition(SATA model)

SATA has receivers and drivers to be connected to Tx+/- and Rx +/- Serial data signal defines the signal names of I/O connector pin and signal name.

	No.	Plug Connector pin definition		Signal	I/O
Signal	S1	GND	2nd mate	Gnd	
	S2	A+	Differential signal A from Phy	RX+	Input
	S3	A-		RX-	Input
	S4	Gnd	2nd mate	Gnd	
	S5	B-	Differential signal B from Phy	TX-	Output
	S6	B+		TX+	Output
	S7	Gnd	2nd mate	Gnd	
Key and spacing separate signal and power segments					
Power	P1	V33	3.3V power	3.3V	
	P2	V33	3.3V power	3.3V	
	P3	V33	3.3V power, pre-charge, 2nd Mate	3.3V	
	P4	Gnd	1st mate	Gnd	
	P5	Gnd	2nd mate	Gnd	
	P6	Gnd	2nd mate	Gnd	
	P7	V5	5V power,pre-charge,2nd Mate	5V	
	P8	V5	5V power	5V	
	P9	V5	5V power	5V	
	P10	Gnd	2nd mate	Gnd	
	P11	Reserved	Support staggered spin-up and LED activity	Reserve	
	P12	Gnd	1st mate	Gnd	
	P13	V12	12V power,pre-chage,2nd mate	V12	
	P14	V12	12V power	V12	
	P15	V12	12V power	V12	

Table 13 Interface connector pins and I/O signals

5.1.4.1 TX+ / TX-

These signals are the outbound high-speed differential signals that are connected to the serial ATA cable

5.1.4.2 RX+ / RX-

These signals are the inbound high-speed differential signals that are connected to the serial ATA cable.

The following standard shall be referenced about signal specifications.
Serial ATA: High Speed Serialized AT Attachment Revision 1.0a 7-January -2003

5.1.5 Out of band signaling(SATA model)

Figure 5 shows the timing of COMRESET, COMINIT and COMWAKE.

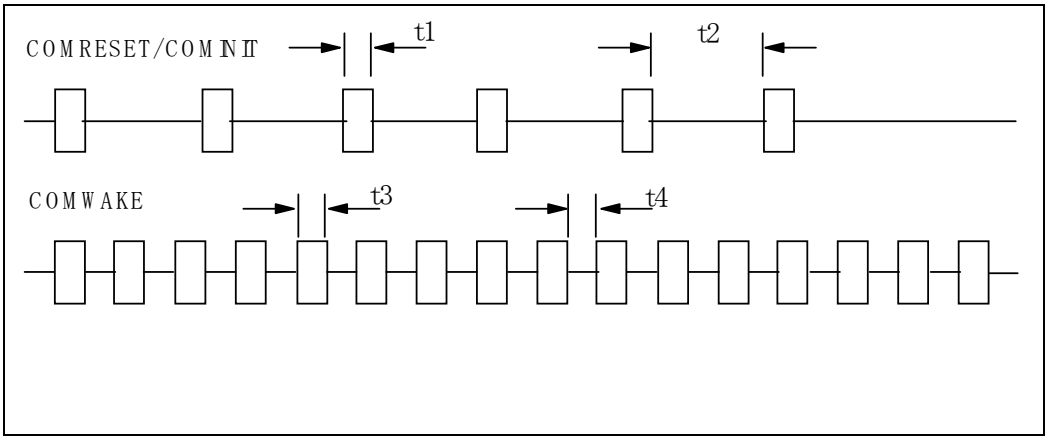


Figure 5 the timing of COMRESET, COMINIT and COMWAKE

	PARAMETER DESCRIPTION	Nominal (ns)
t1	ALIGN primitives	106.7
t2	Spacing	320
t3	ALIGN primitives	106.7
t4	Psacing	106.7

Table 14 Parameter descriptions

5.2 Signal timings

5.2.1 Reset timings

Drive reset timing.

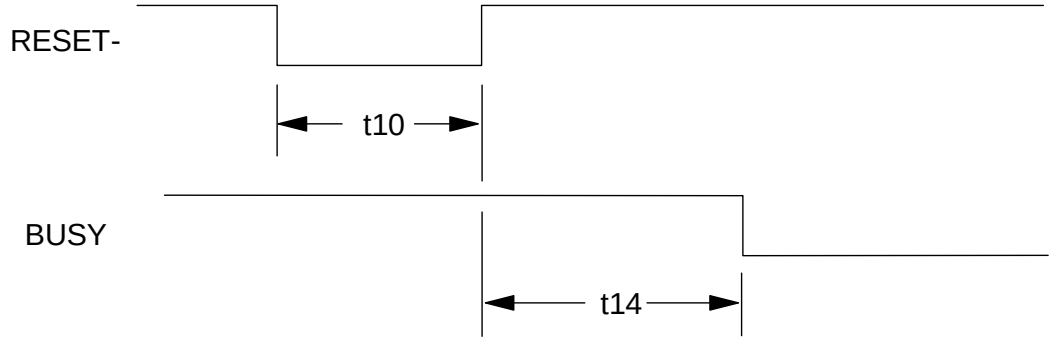


Figure 6 System reset timing chart

	PARAMETER DESCRIPTION	Min (usec)	Max (sec)
t10	RESET low width	25	
t14	RESET high to not BUSY	–	31

Table 15 System reset timing

5.2.2 PIO timings

The PIO cycle timings meet Mode 4 of the ATA/ATAPI-6 description.

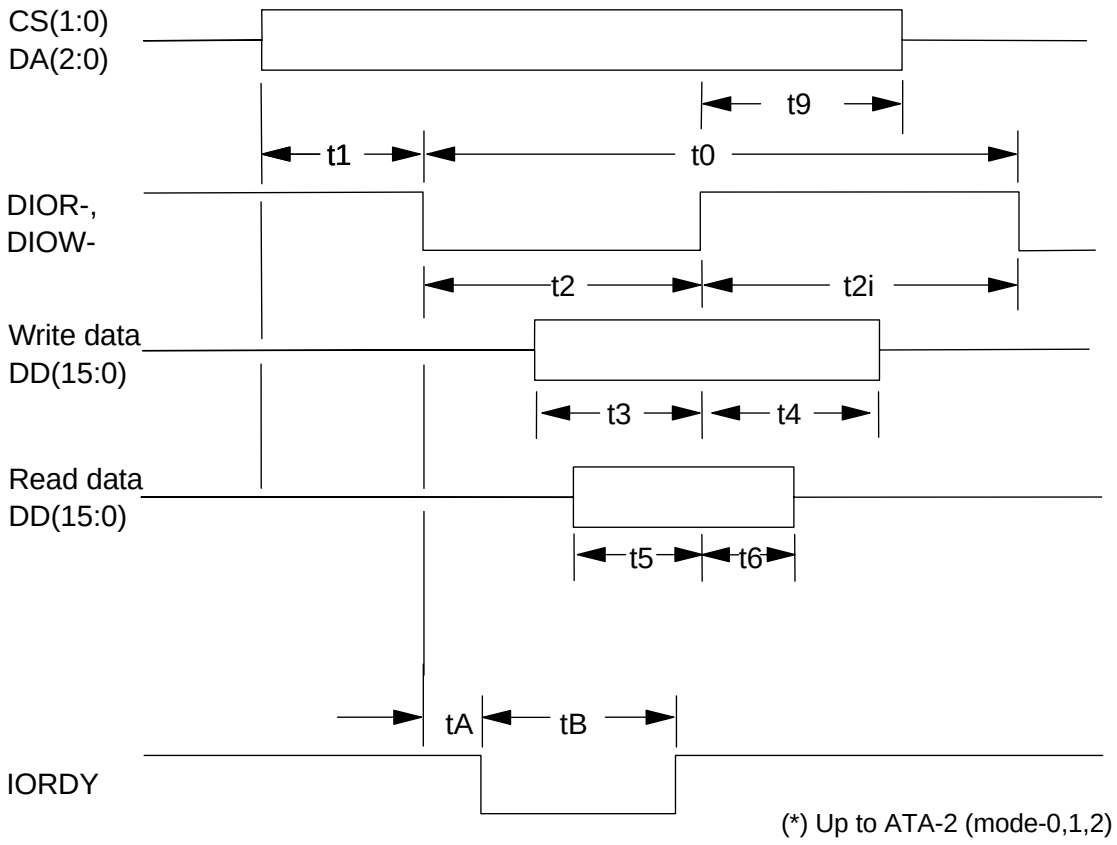


Figure 7 PIO cycle timings chart

	PARAMETER DESCRIPTION	MIN (ns)	MAX (ns)
t0	Cycle time	120	–
t1	Address valid to DIOR-/DIOW– setup	25	–
t2	DIOR–/DIOW– pulse width	70	–
t2i	DIOR–/DIOW– recovery time	25	–
t3	DIOW– data setup	20	–
t4	DIOW– data hold	10	–
t5	DIOR– data setup	20	–
t6	DIOR– data hold	5	–
t9	DIOR–/DIOW– to address valid hold	10	-
tA	IORDY set up time	–	35
tB	IORDY pulse width	–	1250

Table 16 PIO cycle timings

5.2.2.1 Write DRQ interval time

For write sectors and write multiple operations 3.8 μs is inserted from the end of negation of the DRQ bit until setting of the next DRQ bit.

5.2.2.2 Read DRQ interval time

For read sectors and read multiple operations the interval from the end of negation of the DRQ bit until setting of the next DRQ bit is as follows:

- In the event that a host reads the status register only before the sector or block transfer DRQ interval, the DRQ interval 4.2 μs
- In the event that a host reads the status register after or both before and after the sector or block transfer, the DRQ interval is 11.5 μs

5.2.3 Multiword DMA timings

The Multiword DMA timing meets Mode 2 of the ATA/ATAPI-6 description.

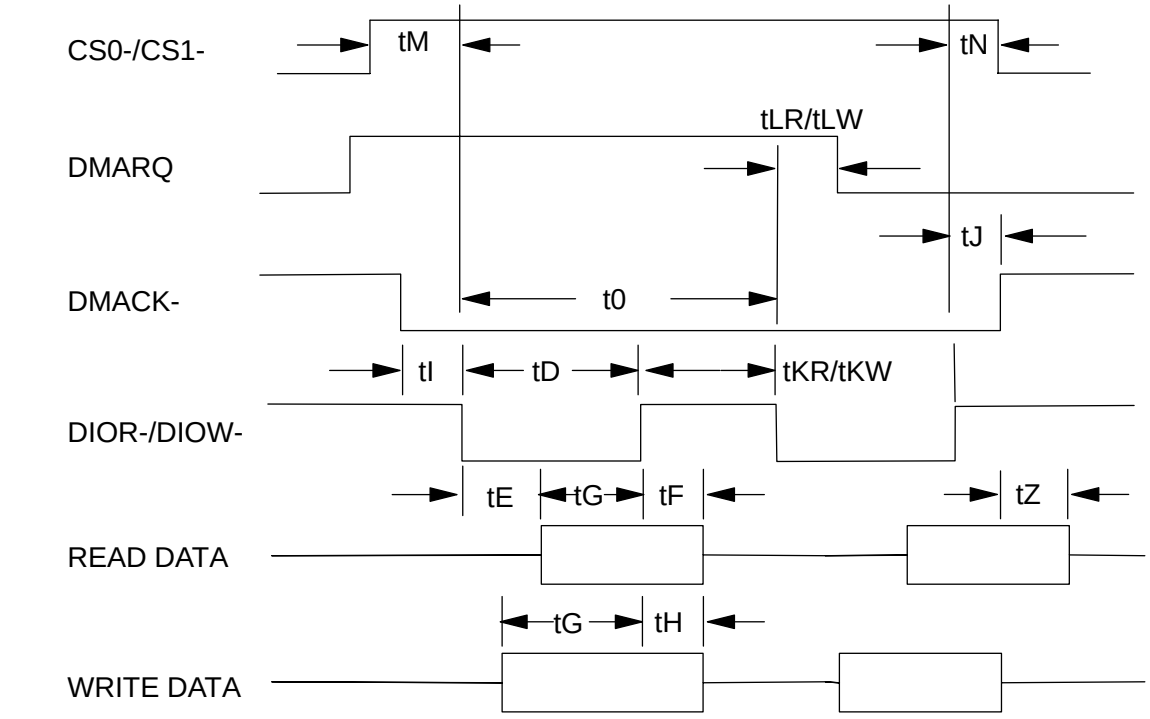


Figure 8 Multiword DMA cycle timing chart

	PARAMETER DESCRIPTION	MIN (ns)	MAX (ns)
t0	Cycle time	120	–
tD	DIOR–/DIOW– asserted pulse width	70	–
tE	DIOR– data access	–	50
tF	DIOR– data hold	5	–
tG	DIOR–/DIOW– data setup	20	–
tH	DIOW– data hold	10	–
tI	DMACK– to –DIOR–/DIOW– setup	0	–
tJ	DIOR–/DIOW– to DMACK– hold	5	–
tKR/tKW	DIOR–/DIOW– negated pulse width	25	–
tLR/tLW	DIOR–/DIOW– to DMARQ– delay	–	35
tM	CS (1:0) valid to DIOR–/DIOW–	25	–
tN	CS (1:0) hold	10	–
tZ	DMACK– to read data released	–	25

Table 17 Multiword DMA cycle timings

5.2.4 Ultra DMA timings

The Ultra DMA timing meets Mode 0,1,2,3 4, and 5 of the Ultra DMA Protocol.

5.2.4.1 Initiating Read DMA

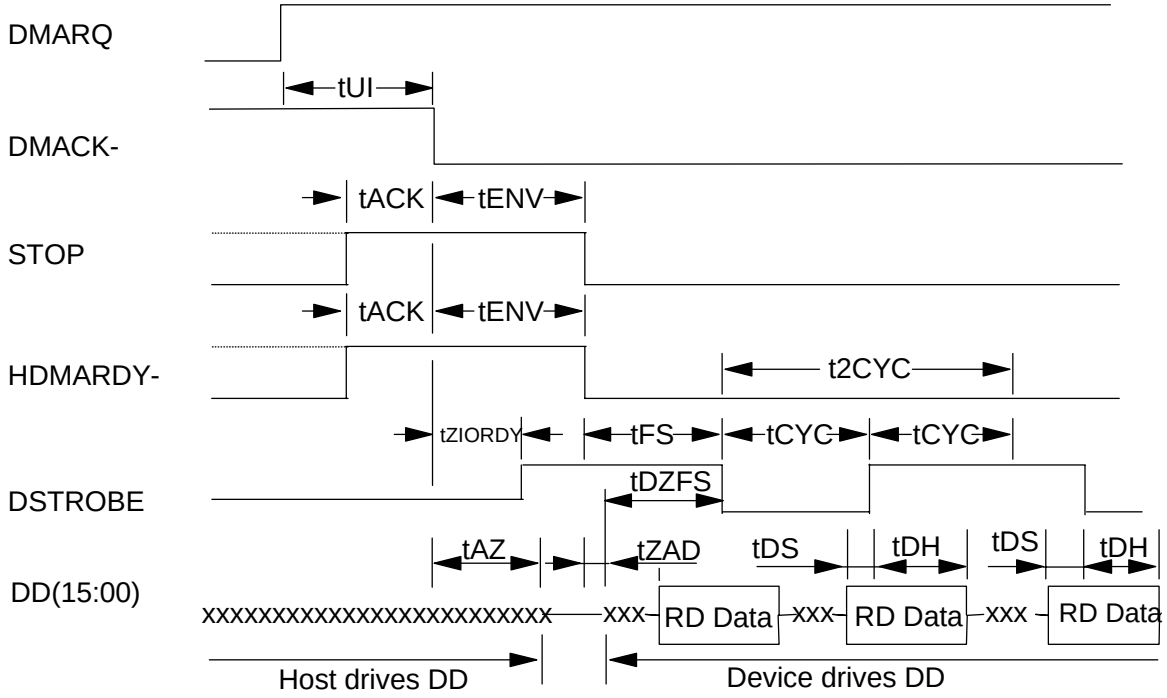


Figure 9 Ultra DMA cycle timing chart (Initiating Read)

	PARAMETER DESCRIPTION (all values in ns)	MODE0		MODE1		MODE2		MODE3		MODE4		MODE5		MODE6	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tUI	Unlimited interlock time	0	–	0	–	0	0	0	–	0	–	0	–	0	–
tACK	Setup time before –DMACK	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tENV	Envelope time	20	70	20	70	20	70	20	55	20	55	20	50	20	50
tZIORDY	Minimum time before driving IORDY	0	–	0	–	0	–	0	–	0	–	0	–	0	–
tFS	First DSTROBE time	0	230	0	200	0	170	0	130	0	120	0	90	0	80
tCYC	Cycle time	112	–	73	–	54	–	39	–	25	–	17	–	13	–
t2CYC	Two cycle time	230	–	153	–	115	–	86	–	57	–	38	–	29	–
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10	–	10	–	10
tZAD	Maximum time allowed for output drivers to assert	0	–	0	–	0	–	0	–	0	–	0	–	0	–
tDS	Data setup time (at host)	15	–	10	–	7	–	7	–	5	–	4	–	2.6	–
tDH	Data hold time (at host)	5	–	5	–	5	–	5	–	5	–	4.6	–	3.5	–
tDZFS	Time from data output released-to-driving until the first transition of critical timing	70	-	48	-	31	-	20	-	6.7	-	25	-	17.5	-

Table 18 Ultra DMA cycle timings (Initiating Read)

5.2.4.2 Host Pausing Read DMA

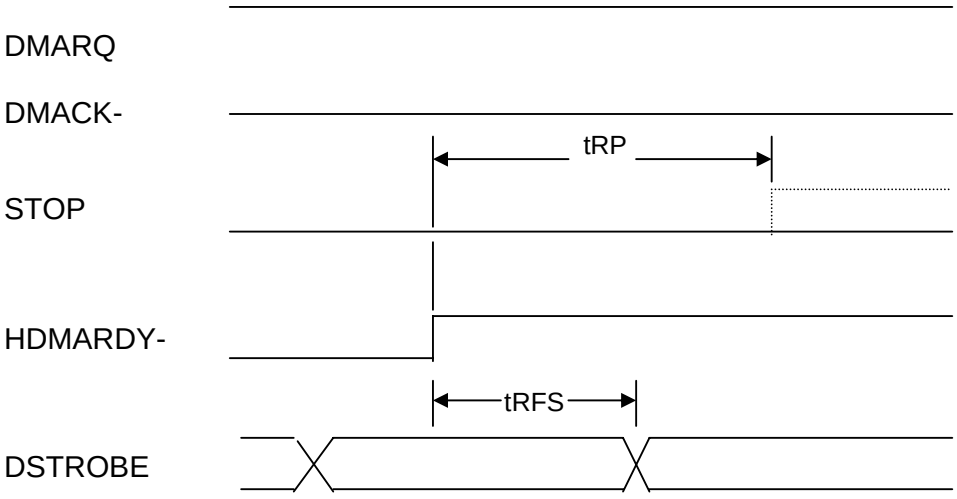


Figure 10 Ultra DMA cycle timing chart (Host pausing Read)

	PARAMETER DESCRIPTION (all values in ns)	MODE0		MODE1		MODE2		MODE3		MODE4		MODE5		MODE6	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–	85	–	85	–
tRFS	HDMARDY– to final DSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50		50

Table 19 Ultra DMA cycle timings (Host pausing Read)

5.2.4.3 Host Terminating Read DMA

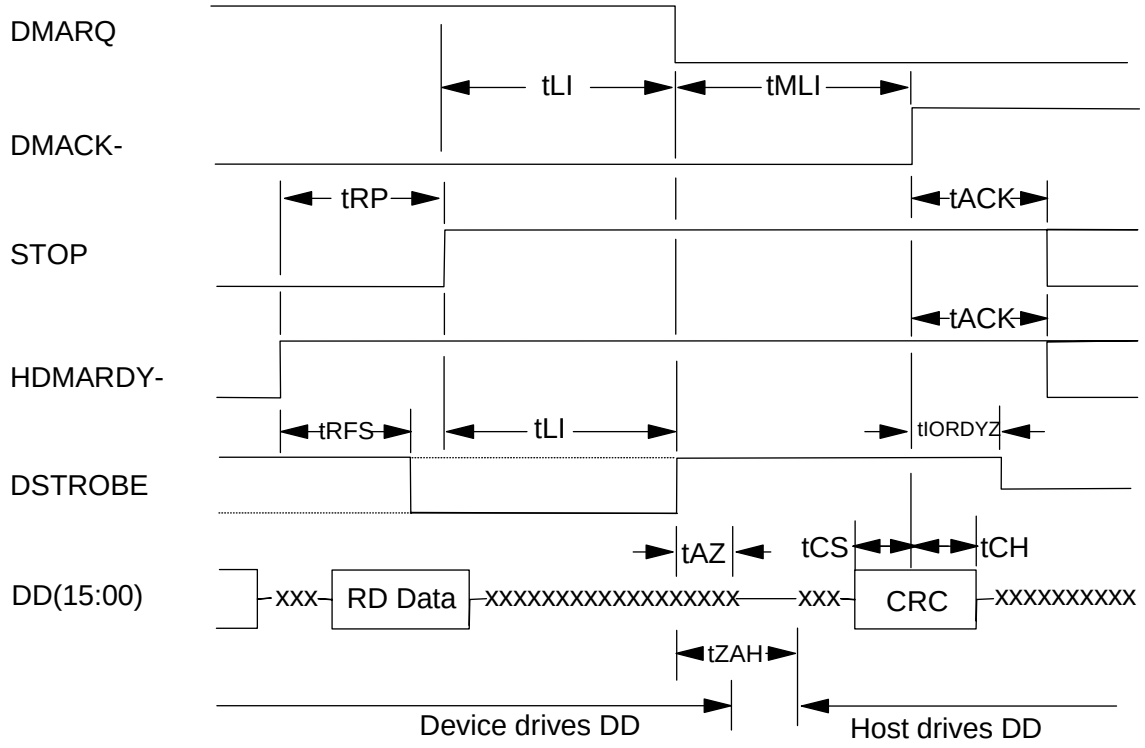


Figure 11 Ultra DMA cycle timing chart (Host terminating Read)

	PARAMETER DESCRIPTION (all values in ns)	MODE0		MODE1		MODE2		MODE3		MODE4		MODE5		MODE6	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tRFS	HDMARDY– to final DSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50	–	50
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–	85	–	85	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75	0	60
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10	–	10	–	10
tZAH	Minimum delay time required for output	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tMLI	Interlocking time with minimum	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time (at device side)	15	–	10	–	7	–	7	–	5	–	5	–	5	–
tCH	CRC word hold time (at device side)	5	–	5	–	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK –	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20	–	20

Table 20 Ultra DMA cycle timings (Host terminating Read)

5.2.4.4 Device Terminating Read DMA

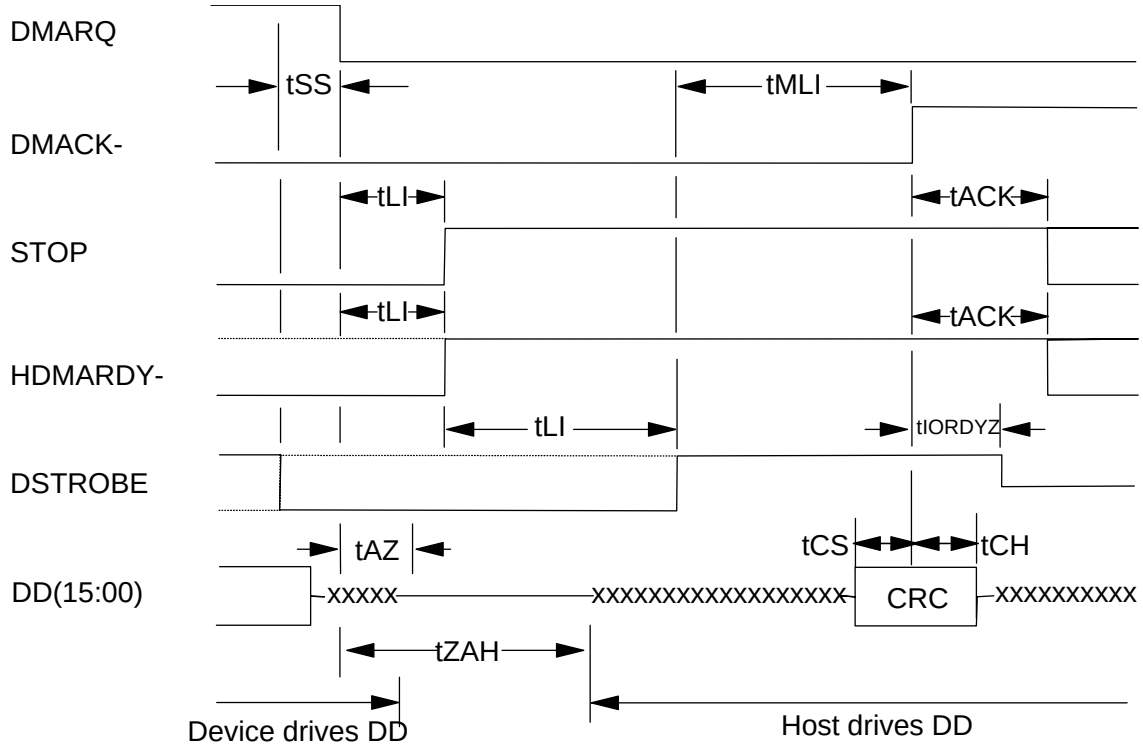


Figure 12 Ultra DMA cycle timing chart (Device terminating Read)

	PARAMETER DESCRIPTION (all values in ns)	MODE0		MODE1		MODE2		MODE3		MODE4		MODE5		MODE6	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tSS	Time from DSTROBE edge to negation of DMARQ	50	–	50	–	50	–	50	–	50	–	50	–	50	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75	0	60
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10	–	10	–	10
tZAH	Minimum delay time required for output	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time (at device side)	15	–	10	–	7	–	7	–	5	–	5	–	5	–
tCH	CRC word hold time (at device side)	5	–	5	–	5	–	5	–	5	–	5	–	5	–
tACK	Hold time after DMACK–	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20	–	20

Table 21 Ultra DMA cycle timings (Device Terminating Read)

5.2.4.5 Initiating Write DMA

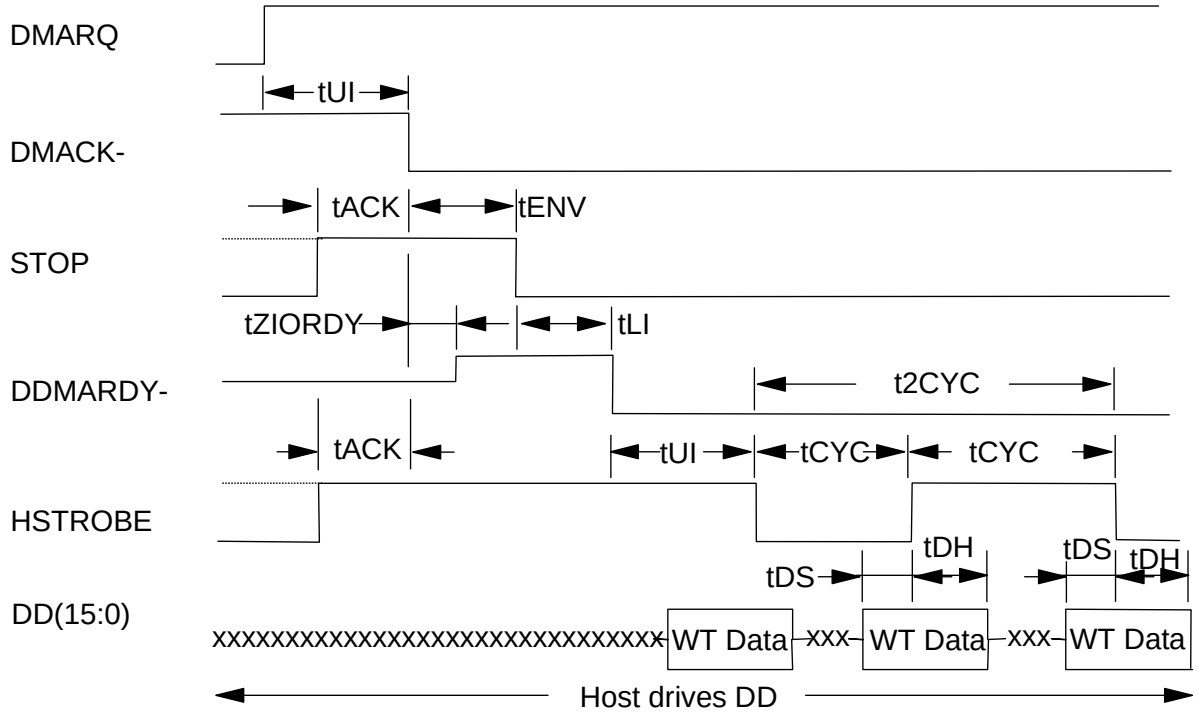


Figure 13 Ultra DMA cycle timing chart (Initiating Write)

	PARAMETER DESCRIPTION (all values in ns)	MODE0		MODE1		MODE2		MODE3		MODE4		MODE5		MODE6	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tUI	Unlimited interlock time	0	–	0	–	0	–	0	–	0	–	0	–	0	–
tACK	Setup time before DMACK–	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tENV	Envelope time	20	70	20	70	20	70	20	55	20	55	20	50	20	50
tZIORDY	Minimum time before driving IORDY	0	–	0	–	0	–	0	–	0	–	0	–	0	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75	0	60
tCYC	Cycle time	112	–	73	–	54	–	39	–	25	–	16.8	–	13.0	–
t2CYC	Two Cycle time	230	–	154	–	115	–	86	–	57	–	38	–	29	–
tDS	Data setup time (at device side)	15	–	10	–	7	–	7	–	5	–	4	–	2.6	–
tDH	Data hold time (at device side)	5	–	5	–	5	–	5	–	5	–	4.6	–	3.5	–

Table 22 Ultra DMA cycle timings (Initiating Write)

5.2.4.6 Device Pausing Write DMA

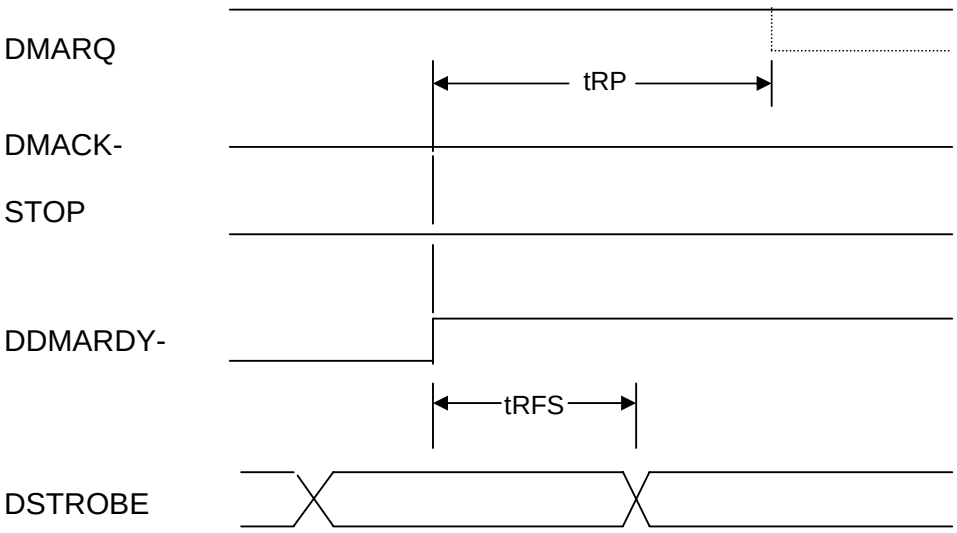


Figure 14 Ultra DMA cycle timing chart (Device Pausing Write)

	PARAMETER DESCRIPTION (all values in ns)	MODE0		MODE1		MODE2		MODE3		MODE4		MODE5		MODE6	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	-	85	–	85	–
tRFS	DDMARDY– to final HSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50	–	50

Table 23 Ultra DMA cycle timings (Device Pausing Write)

5.2.4.7 Device Terminating Write DMA

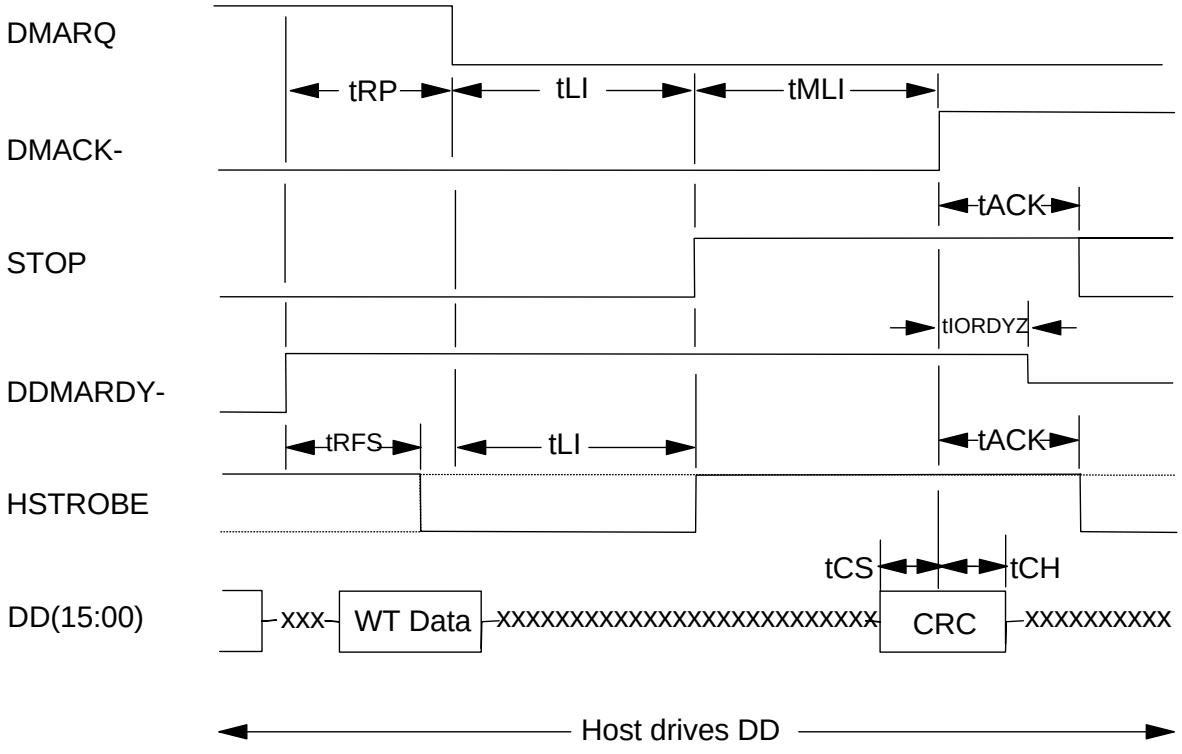


Figure 15 Ultra DMA cycle timing chart (Device Terminating Write)

	PARAMETER DESCRIPTION (all values in ns)	MODE0		MODE1		MODE2		MODE3		MODE4		MODE5		MODE6	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tRFS	DDMARDY to final HSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50	–	50
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–	85	–	85	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75	0	60
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time (at device side)	15	–	10	–	7	–	7	–	5	–	5	–	5	–
tCH	CRC word hold time (at device side)	5	–	5	–	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for –DMACK	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20	–	20

Table 24 Ultra DMA cycle timings (Device terminating Write)

5.2.4.8 Host Terminating Write DMA

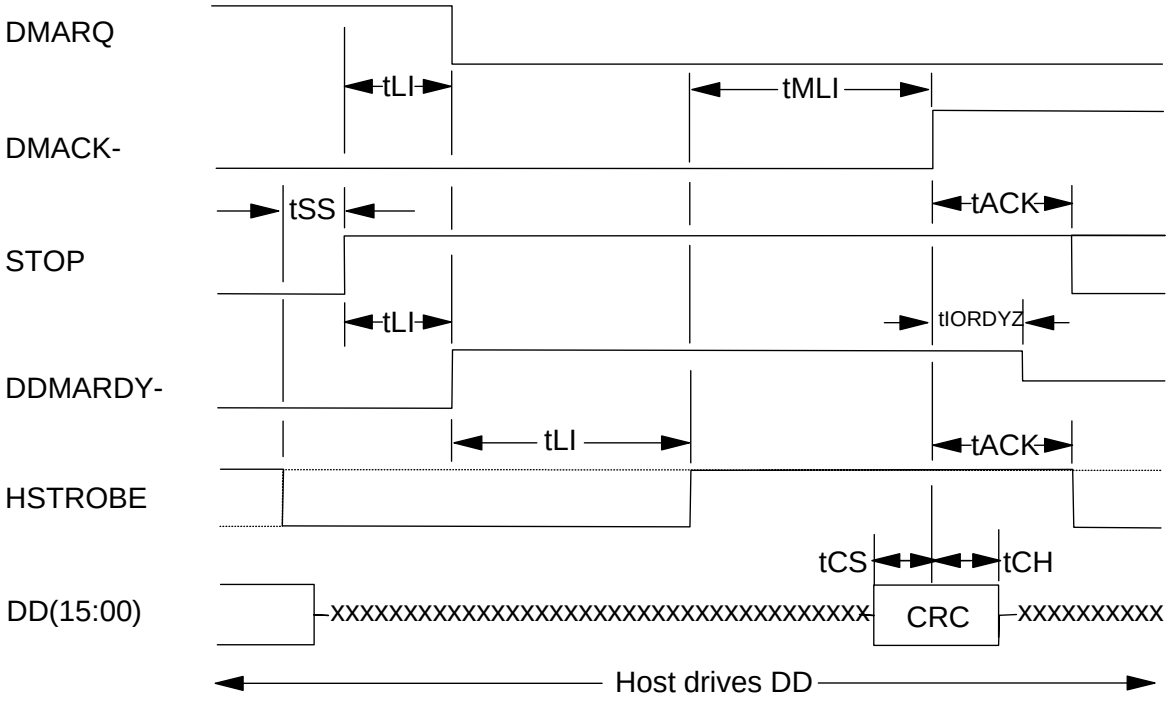


Figure 16 Ultra DMA cycle timing chart (Host Terminating Write)

	PARAMETER DESCRIPTION (all values in ns)	MODE0		MODE1		MODE2		MODE3		MODE4		MODE5		MODE6	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tSS	Time from HSTROBE to edge assertion of STOP	50	–	50	–	50	–	50	–	50	–	50	–	50	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75	0	60
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time (at device side)	15	–	10	–	7	–	7	–	5	–	5	–	5	–
tCH	CRC word hold time (at device side)	5	–	5	–	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK–	20	–	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20	–	20

Table 25 Ultra DMA cycle timings (Host Terminating Write)

5.2.5 Addressing of registers

The host addresses the drive through a set of registers called the Task File. These registers are mapped into the I/ O space of the host. Two chip select lines (CS0– and CS1–) and three address lines (DA0-02) are used to select one of these registers, while a DIOR– or DIOW– is provided at the specified time.

The CS0– is used to address Command Block registers. while the CS1– is used to address Control Block registers.

The following table shows the I/ O address map.

CS0–	CS1–	DA2	DA1	DA0	DIOR– = 0 (Read)	DIOW– = 0 (Write)
					Command Block Registers	
0	1	0	0	0	Data Reg.	Data Reg.
0	1	0	0	1	Error Reg.	Features Reg.
0	1	0	1	0	Sector count Reg.	Sector count Reg.
0	1	0	1	1	Sector number Reg.	Sector number Reg.
0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
0	1	1	1	0	Device/Head Reg.	Device/Head Reg.
0	1	1	1	1	Status Reg.	Command Reg.
					Control Block Registers	
1	0	1	1	0	Alt. Status Reg.	Device control Reg.

Table 26 I/O address map

Note: "Addr" field is shown as an example.

During DMA operation (from writing to the command register until an interrupt) not all registers are accessible. For example, the host is not supposed to read status register contents before interrupt (the value is invalid).

5.2.6 Cabling

The maximum cable length from the host system to the drive plus circuit pattern length in the host system shall not exceed 18 inches.

For higher data transfer application (>8.3 MB/s) a modification in the system design is recommended to reduce cable noise and cross-talk, such as a shorter cable, bus termination, or a shielded cable.

For systems operating with Ultra DMA mode 3, 4, and 5, 80-conductor ATA cable assembly shall be used.

5.3 Jumper settings(PATA model)

5.3.1 Jumper pin location

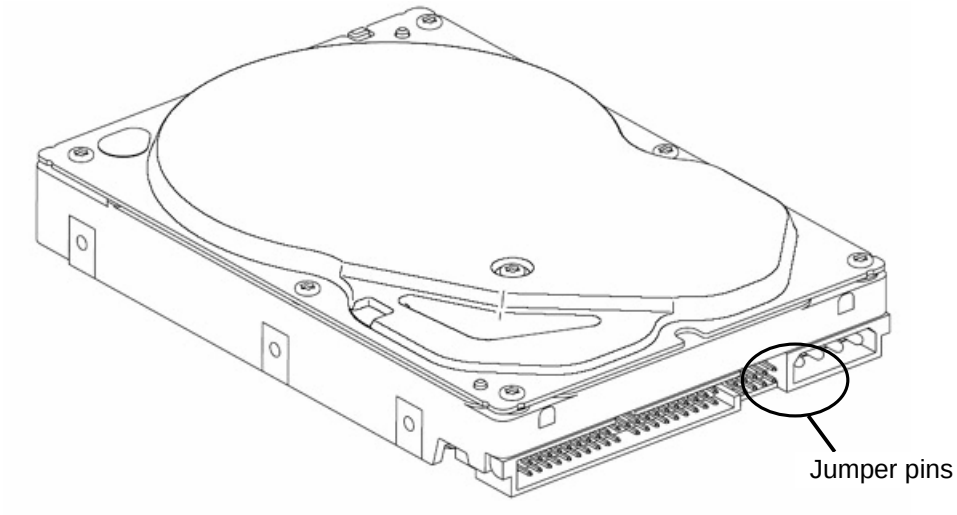


Figure 17 Jumper pin location

5.3.2 Jumper pin identification

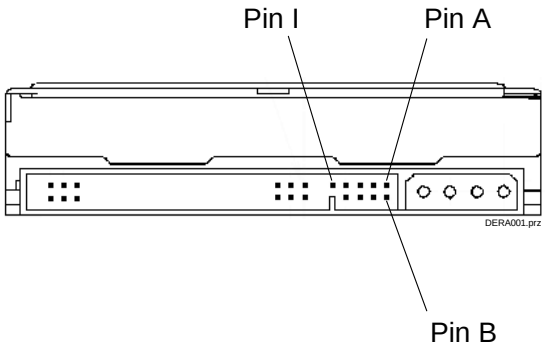


Figure 18 Jumper pin identification

5.3.3 Jumper pin assignment

There are four jumper settings as shown in the following sections:

- 16 logical head default (normal use)
- 15 logical head default
- 32 GB clip
- Power up in standby

Within each of these four jumper settings the pin assignment selects *Device 0, Device 1, Cable Selection*, or *Device 1 Slave Present* as shown in the following figures.

The Device 0 setting automatically recognizes device 1 if it is present.

The Device 1 Slave Present setting is for a slave device that does not comply with the ATA specification.

Note: In conventional terminology "Device 0" designates a *Master* and "Device 1" designates a *Slave*.

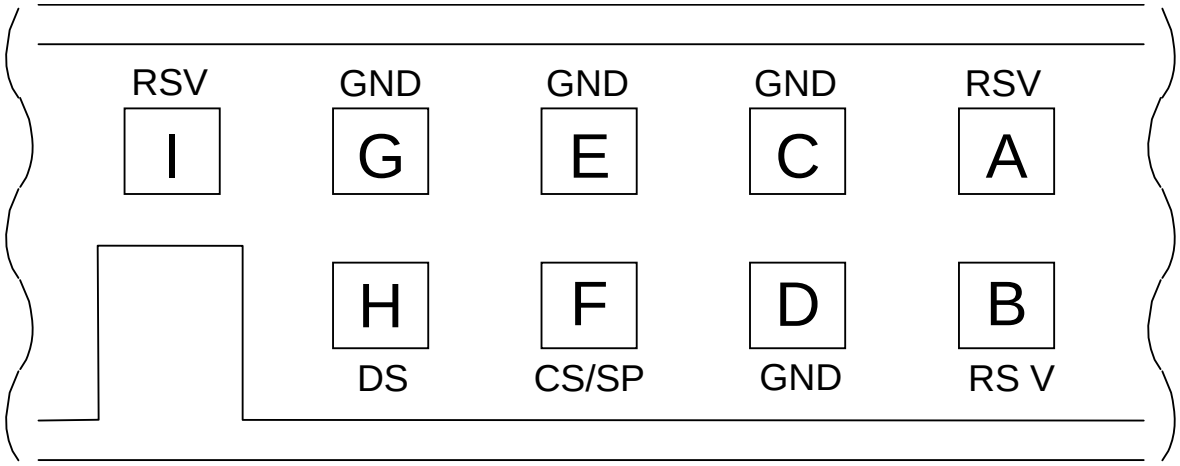


Figure 49. Jumper pin assignment

5.3.4 Jumper positions

5.3.4.1 16 logical head default (normal use)

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device 1 (Slave) Present.

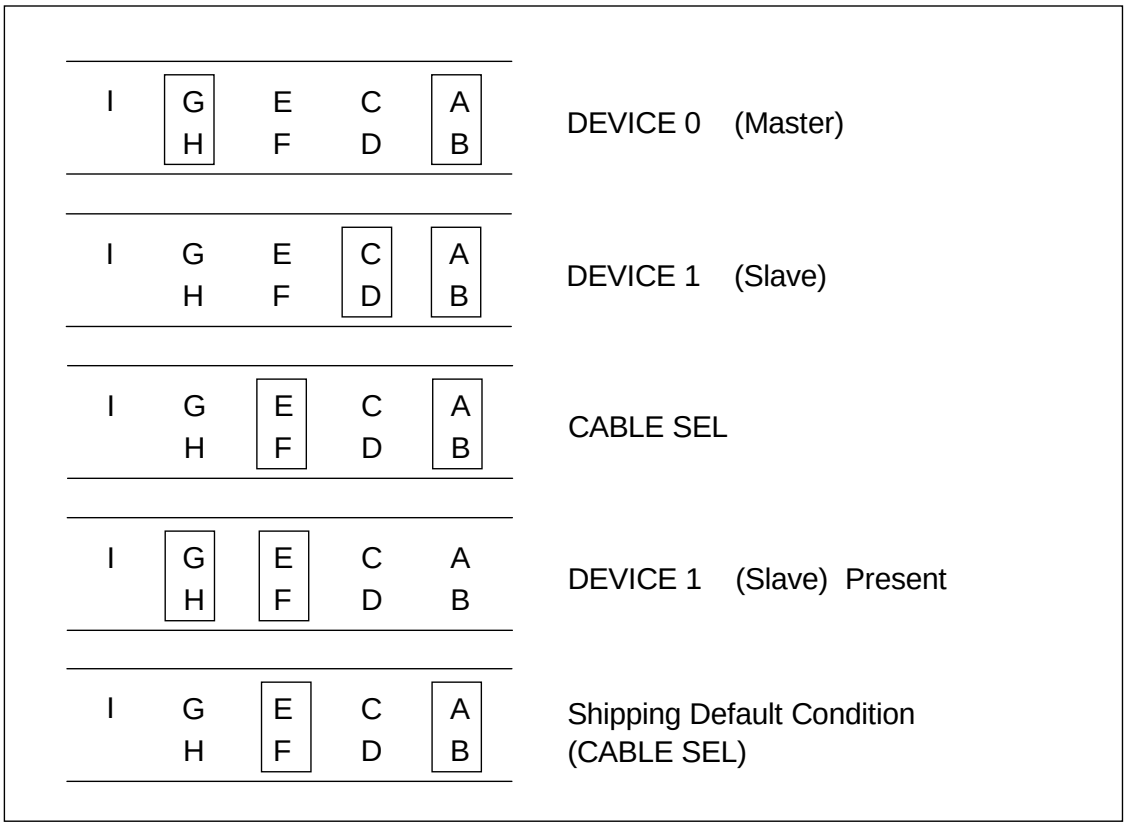


Figure 19 Jumper positions for normal use

Notes:

1. *To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In the CSEL mode the drive address is determined by AT interface signal #28 CSEL as follows:*
   - *When CSEL is grounded or at a low level, the drive address is 0 (Device 0).*
   - *When CSEL is open or at a high level, the drive address is 1 (Device 1).*
2. *In CSEL mode, installing or removing the jumper blocks at A-B or C-D position does not affect any selection of Device or Cable Selection mode.*
3. *The shipping default position is Cable Select position.*

5.3.4.2 15 logical head default

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device 1 (Slave) Present setting 15 logical heads instead of default 16 logical head models.

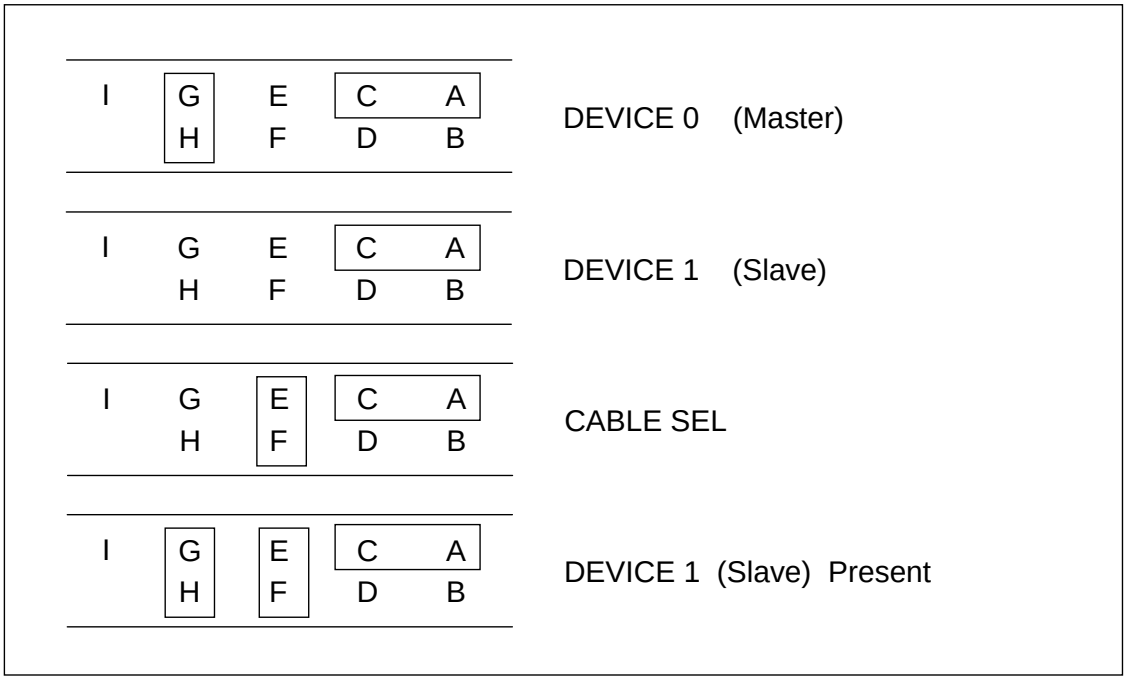


Figure 20 Jumper positions for 15 logical head default

Notes:

1. *To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In the CSEL mode, the drive address is determined by AT interface signal #28 CSEL as follows:*
   - *When CSEL is grounded or at a low level, the drive address is 0 (Device 0).*
   - *When CSEL is open or at a high level, the drive address is 1 (Device 1).*
2. *In CSEL mode, installing or removing the jumper blocks at A-C or B-D position does not affect any selection of Device or Cable Selection mode.*

5.3.4.3 Capacity clip to 32GB

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device 1 (Slave) Present while setting the drive capacity down either to 32GB for the purpose of compatibility.

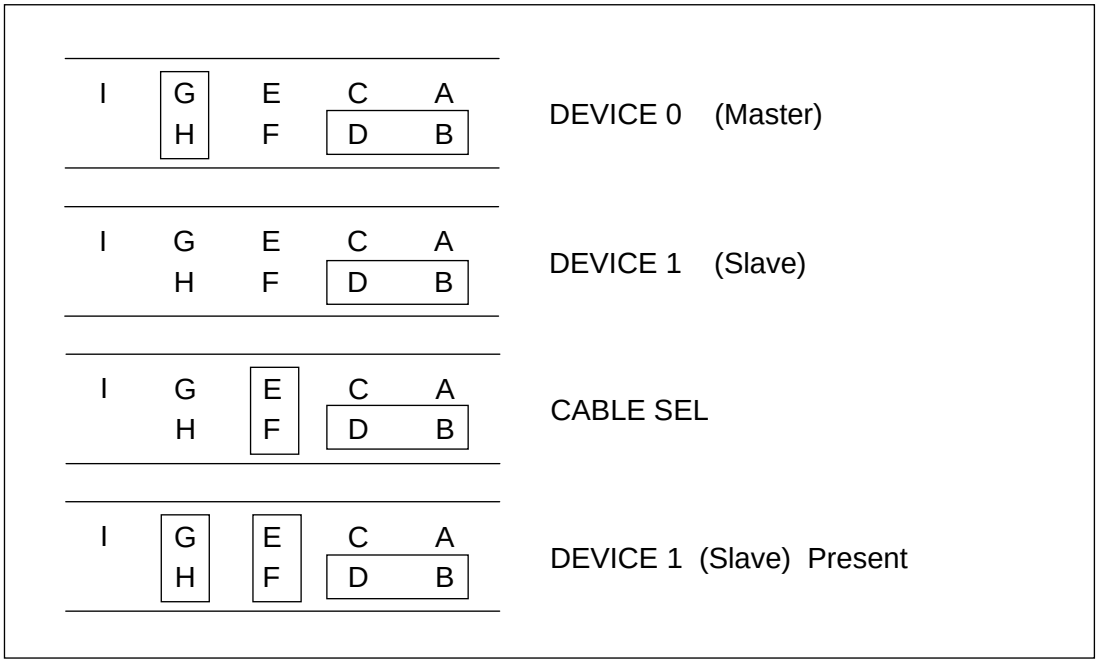


Figure 21 Jumper positions for capacity clip to 32GB

Notes:

The jumper setting acts as a 32GB clip which clips the LBA to 66055248. The CHS is unchanged from the factory default of 16383/16/63.

5.3.4.4 Power Up In Standby

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device 1 (Slave) Present to enable Power Up In Standby.

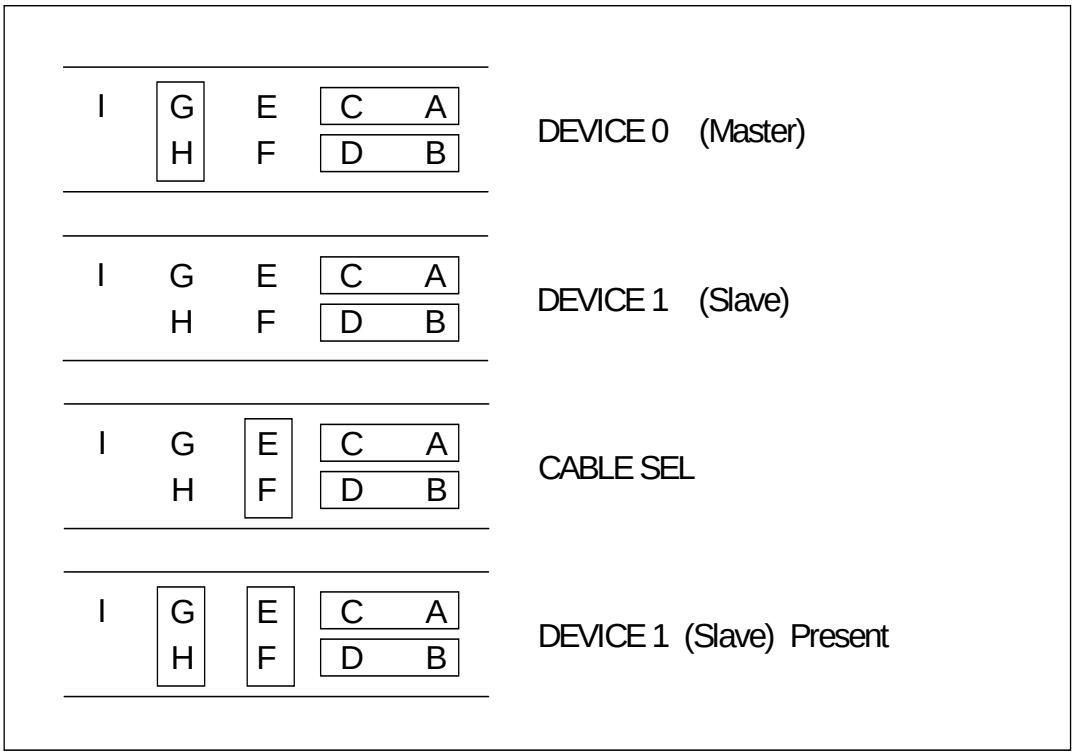


Figure 22 Jumper settings for Disabling Auto Spin

Notes:

1. *These jumper settings are used for limiting power supply current when multiple drives are used.*
2. *Command to spin up is SET FEATURES (subcommand 07h). Refer to 10.37 Set Features.*
3. *To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In CSEL mode, the drive address is determined by AT interface signal #28 as follows:*
   - *When CSEL is grounded or at a low level, the drive address is 0 (Device 0).*
   - *When CSEL is open or at a high level, the drive address is 1 (Device 1).*

5.4 Environment

5.4.1 Temperature and humidity

Operating conditions	
Temperature	0 to 60°C
Relative humidity	8 to 90% non-condensing
Maximum wet bulb temperature	29.4°C non-condensing
Maximum temperature gradient	20°C/Hour
Altitude	–300 to 3,048 m
Non-Op conditions	
Temperature	-40 to 70°C
Relative humidity	5 to 95% non-condensing
Maximum wet bulb temperature	35°C non-condensing
Maximum temperature gradient	30°C/Hour
Altitude	–300 to 12,000 m

Table 27 Temperature and humidity

Notes:

1. *The system is responsible for providing sufficient ventilation to maintain a surface temperature below 65°C at the center of the top cover of the drive.*
2. *Non condensing conditions should be maintained at any time.*
3. *Maximum storage period within shipping package is one year,*

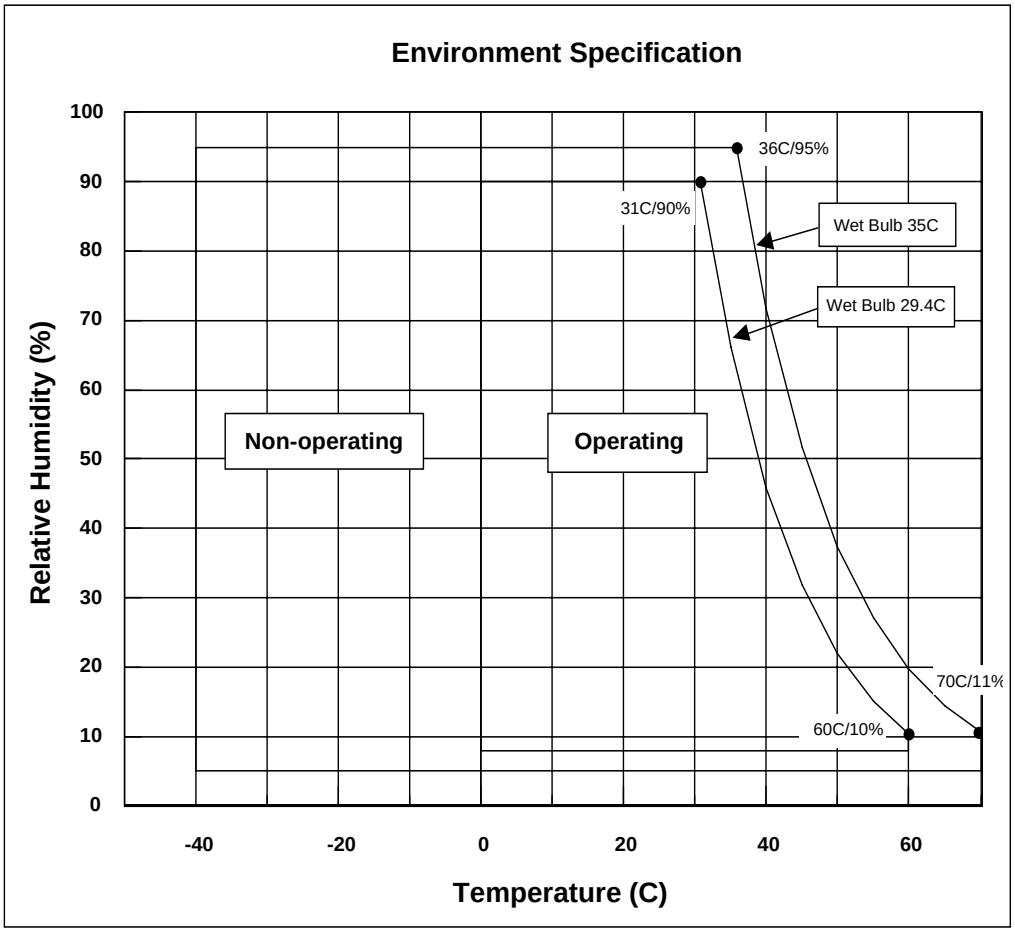


Figure 23 Limits of temperature and humidity

Note: Storage temperature range is 0 to 70°C

5.4.2 Corrosion test

The drive shows no sign of corrosion inside and outside of the hard disk assembly and is functional after being subjected to seven days at 50°C with 90% relative humidity.

5.5 DC power requirements

Damage to the drive electronics may result if the power supply cable is connected or disconnected to the legacy power connector while power is being applied to the drive (no hot plug/unplug is allowed). If SATA power supply cable is connected or disconnected to the SATA power connector, hot plug/unplug is allowed.

5.5.1 Input voltage

Input voltage	During run and spin up	Absolute max spike voltage	Supply rise time
+5 Volts Supply	5V ± 5%	–0.3 to 5.5V	0 to 5sec
+12 Volts Supply	12V ±10%	–0.3 to 15.0V	0 to 5sec

Table 28 Input voltage

Caution** : To avoid damage to the drive electronics, **power supply voltage spikes must not exceed specifications.

5.5.2 Power supply current (typical)

Power supply current of 2 Disk PATA models (values in milliamps. RMS)	**+5 Volts [mA]**		**+12 Volts [mA]**		**Total** [W]
	Pop Mean	Std Dev	Pop Mean	Std Dev	
Idle average	130	10	320	15	4.5
Idle ripple (peak-to-peak)	200	10	300	20	
Low RPM Idle	80	10	130	15	2.0
Low RPM Idle Ripple	100	10	250	20	
Unload Idle average	80	10	280	15	3.8
Unload Idle Ripple	100	10	300	20	
Random R/W average[1]	240	10	560	15	7.9
Random R/W peak	700	20	1500	40	
Start up (max)	400	20	2000	50	
Standby average	75	10	5	5	0.5
Sleep average	65	10	5	5	0.5

Table 29 Power supply current of 2 Disk PATA models

Except for a peak of less than 100 μs duration.

[1] Random R/W : 40 IOPS / 16 Blocks Random Write and Random Read

Power supply current of 1 Disk PATA models (values in milliamps. RMS)	**+5 Volts [mA]**		**+12 Volts [mA]**		**Total** [W]
	Pop Mean	Std Dev	Pop Mean	Std Dev	
Idle average	130	10	220	15	3.3
Idle ripple (peak-to-peak)	200	10	300	20	
Low RPM Idle	80	10	110	15	1.7
Low RPM Idle Ripple	100	10	250	20	
Unload Idle average	80	10	210	15	2.9
Unload Idle Ripple	100	10	300	20	
Random R/W average[1]	240	10	410	15	6.1
Random R/W peak	700	20	1200	40	
Start up (max)	400	20	2000	50	
Standby average	75	10	5	5	0.5
Sleep average	65	10	5	5	0.5

Table 30 Power supply current of 1 Disk PATA models

Except for a peak of less than 100 μs duration
[1] Random R/W : 40 IOPS / 16 Blocks Random Write and Random Read

Power supply current of 2 Disk SATA models *(values in milliamps. RMS)*	**+5 Volts [mA]**		**+12 Volts [mA]**		**Total** [W]
	Pop Mean	Std Dev	Pop Mean	Std Dev	
Idle average	190	10	320	15	4.8
Idle ripple (peak-to-peak)	200	10	300	20	
Low RPM Idle	140	10	130	15	2.3
Low RPM Idle Ripple	100	10	250	20	
Unload Idle average	140	10	280	15	4.1
Unload Idle Ripple	100	10	300	20	
Random R/W average[1]	300	10	560	15	8.2
Random R/W peak	800	20	1500	40	
Start up (max)	500	20	2000	50	
Standby average	135	10	5	5	0.8
Sleep average	130	10	5	5	0.8

Table 31 Power supply current of 2 Disk SATA models

Except for a peak of less than 100 μs duration
[1] Random R/W : 40 IOPS / 16 Blocks Random Write and Random Read

Power supply current of 1 Disk SATA models *(values in milliamps. RMS)*	**+5 Volts [mA]**		**+12 Volts [mA]**		**Total** [W]
	Pop Mean	Std Dev	Pop Mean	Std Dev	
Idle average	190	10	220	15	3.6
Idle ripple (peak-to-peak)	200	10	300	20	
Low RPM Idle	140	10	110	15	2.0
Low RPM Idle Ripple	100	10	250	20	
Unload Idle average	140	10	210	15	3.2
Unload Idle Ripple	100	10	300	20	
Random R/W average[1]	300	10	410	15	6.4
Random R/W peak	800	20	1200	40	
Start up (max)	500	20	2000	50	
Standby average	135	10	5	5	0.8
Sleep average	130	10	5	5	0.8

Table 32 Power supply current of 1 Disk SATA models

Except for a peak of less than 100 µs duration

[1] Random R/W : 40 IOPS / 16 Blocks Random Write and Random Read

5.5.3 Power supply generated ripple at drive power connector

	Maximum (mV pp)	**MHz**
+5V DC	150	0-10
+12V DC	250	0-10

Table 33 Power supply generated ripple at drive power connector

During drive start up and seeking 12-volt ripple is generated by the drive (referred to as dynamic loading). If the power of several drives is daisy chained together, the power supply ripple plus the dynamic loading of the other drives must remain within the above regulation tolerance. A common supply with separate power leads to each drive is a more desirable method of power distribution.

To prevent external electrical noise from interfering with the performance of the drive, the drive must be held by four screws in a user system frame which has no electrical level difference at the four screws position and has less than ±300 millivolts peak to peak level difference to the ground of the drive power connector.

5.6 Reliability

5.6.1 Data integrity

No more than one sector is lost at Power loss condition during the write operation when the write cache option is disabled. If the write cache option is active, the data in write cache will be lost. To prevent the loss of customer data, it is recommended that the last write access before power off be issued after setting the write cache off.

5.6.2 Cable noise interference

To avoid any degradation of performance throughput or error rate when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

5.6.3 Start/stop cycles

The drive withstands a minimum of 50,000 start/stop cycles in a 40° C environment and a minimum of 10,000 start/stop cycles in extreme temperature or humidity within the operating range. .

5.6.4 Preventive maintenance

None

5.6.5 Data reliability

Probability of not recovering data is 1 in 10^{14} bits read

ECC On The Fly correction

- 1 Symbol : 10 bits
- No Interleave
- 34 symbol ECC
- This implementation always recovers 16 symbol random erros and a 330-bit continuous burst error

5.6.6 Required Power-Off Sequence

The required BIOS sequence for removing power from the drive is as follows:

Step 1: Issue one of the following commands.

Standby
Standby immediate
Sleep

Note: Do not use the Flush Cache command for the power off sequence because this command does not invoke Unload

Step 2: Wait until the Command Complete status is returned. In a typical case 350 ms are required for the command to finish completion; however, the BIOS time out value needs to be 30 seconds considering error recovery time. Refer to section 11.0 "Timings," on page 266.

Step 3: Terminate power to HDD.

5.7 Mechanical specifications

5.7.1 Physical dimensions

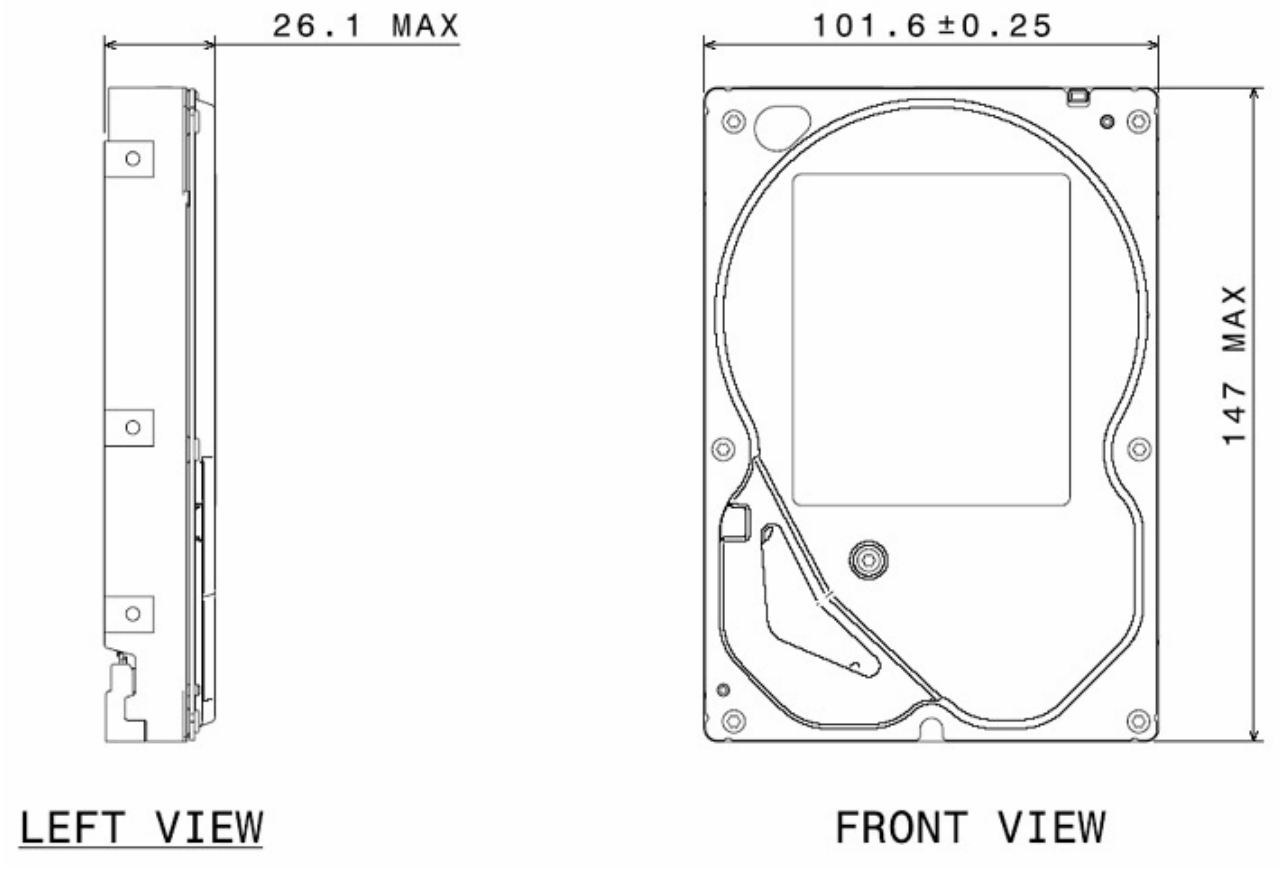


Figure 24 Top and side views with breather hole location and mechanical dimensions

All dimensions are in millimeters.

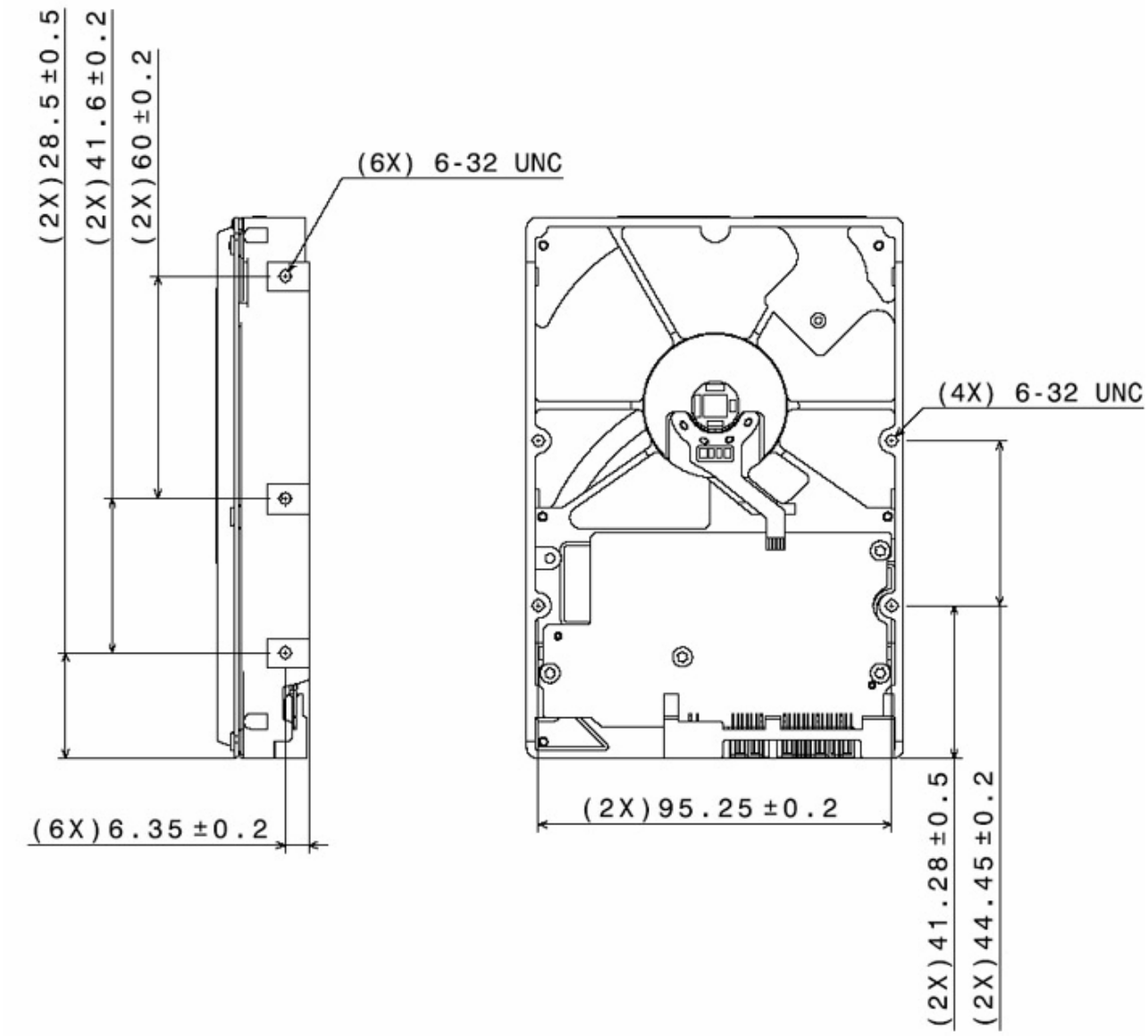


Figure 25 Bottom and side views with mounting hole locations

All dimensions in the above figure are in millimeters.

The breather hole must be kept uncovered in order to keep the air pressure inside of the disk enclosure equal to external air pressure.

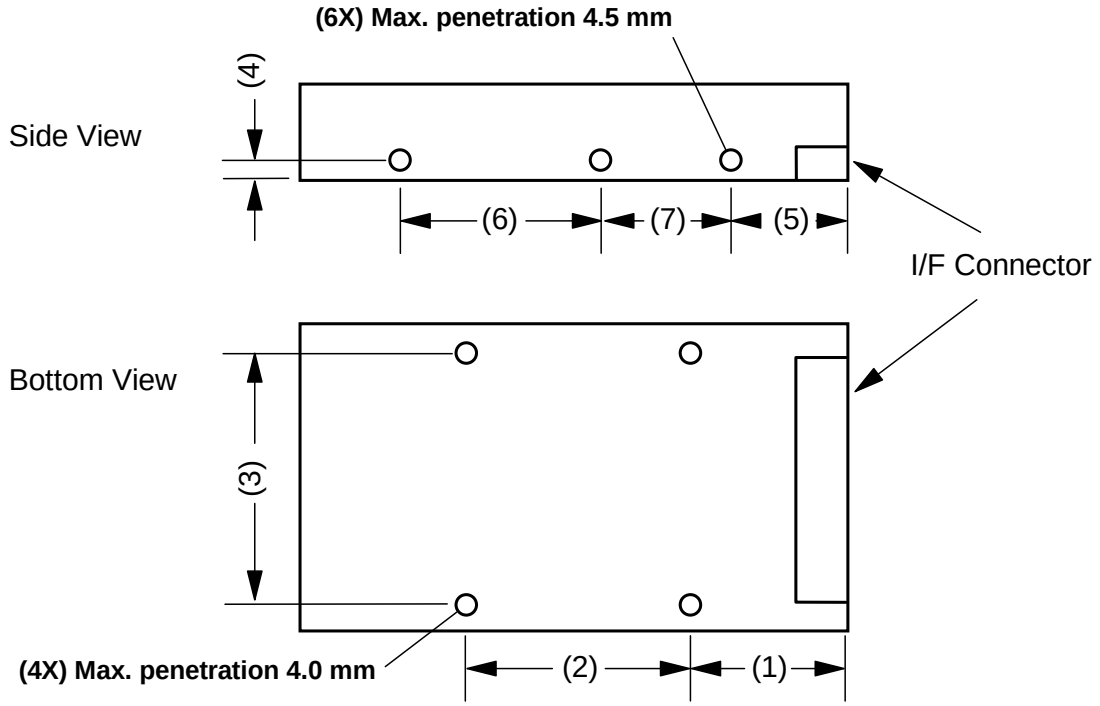
The following table shows the physical dimensions of the drive.

Height (mm)	Width (mm)	Length (mm)	Weight (gram)
26.1 MAX	101.6 ± 0.25	147 MAX	550 MAX

Table 34 Physical Dimensions

5.7.2 Hole locations

The mounting hole location and size for the hard disk drive is shown below.

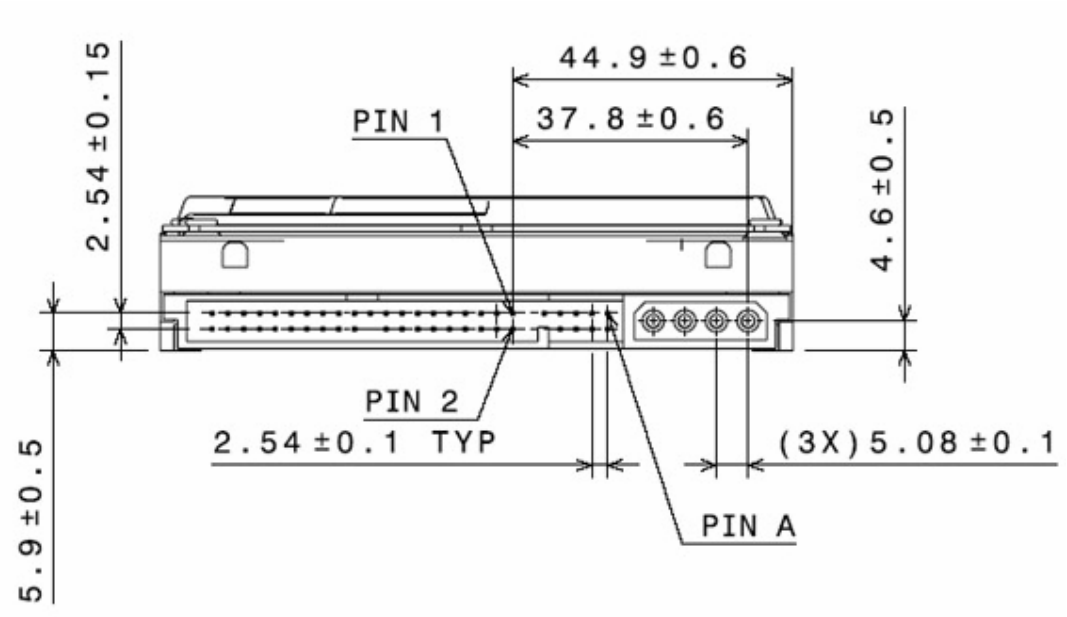


Thread	(1)	(2)	(3)	(4)	(5)	(6)	(7)
6-32UNC	41.28±0.5	44.45±0.2	95.25±0.2	6.35±0.2	28.5±0.5	60.0±0.2	41.6±0.2

Figure 26 Mounting hole locations (all dimensions are in mm)

5.7.3 Connector locations

PATA Model



SATA Model

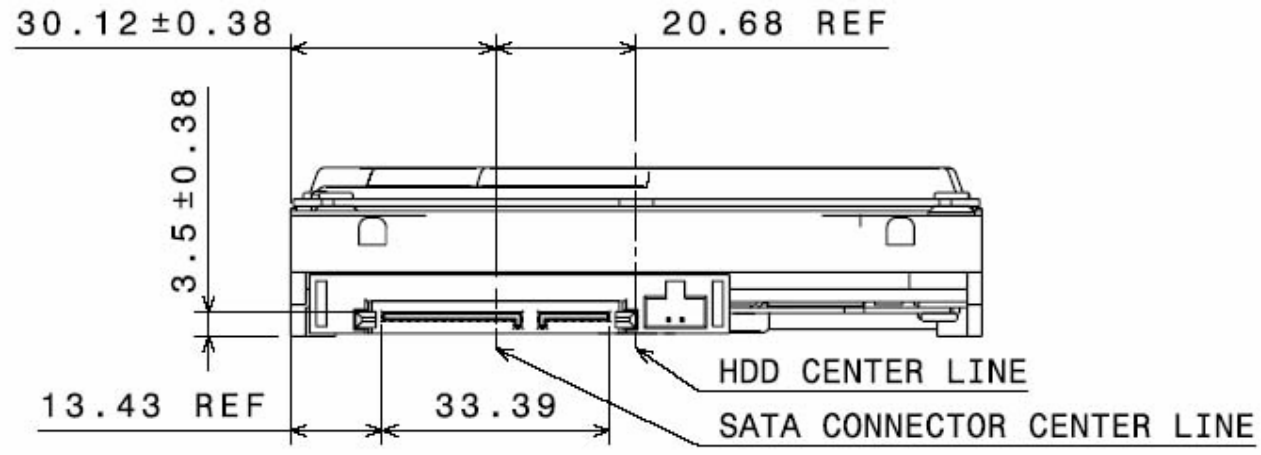


Figure 27 Connector locations

5.7.4 Drive mounting

The drive will operate in all axes (6 directions). Performance and error rate will stay within specification limits if the drive is operated in the other orientations from which it was formatted.

For reliable operation, the drive must be mounted in the system securely enough to prevent excessive motion or vibration of the drive during seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

The recommended mounting screw torque is 0.6 – 1.0 Nm (6-10 Kgf.cm).

The recommended mounting screw depth is 4 mm maximum for bottom and 4.5 mm maximum for horizontal mounting.

Drive level vibration test and shock test are to be conducted with the drive mounted to the table using the bottom four screws.

5.7.5 Heads unload and actuator lock

Heads are moved out from disks (unload) to protect the disk data during shipping, moving, or storage. Upon power down, the heads are automatically unloaded from disk area and the locking mechanism of the head actuator will secure the heads in unload position.

5.8 Vibration and shock

All vibration and shock measurements recorded in this section are made with a drive that has no mounting attachments for the systems. The input power for the measurements is applied to the normal drive mounting points.

5.8.1 Operating vibration

5.8.1.1 Random vibration (Linear)

The test is 30 minutes of random vibration using the power spectral density (PSD) levels shown below in each of three mutually perpendicular axes. The disk drive will operate without non-recoverable errors when subjected to the above random vibration levels.

Frequency	5 Hz	17 Hz	45 Hz	48 Hz	62 Hz	65 Hz	150 Hz	200 Hz	500 Hz	RMS (G)
$x10^{-3}$ $[G^2/Hz]$	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.5	0.5	0.67

Table 35 Random vibration PSD profile break points (operating)

The overall RMS (root mean square) level is 0.67 G.

5.8.1.2 Swept sine vibration (Linear)

The drive will meet the criteria shown below while operating in the specified conditions:

- No errors occur with 0.5 G 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3-minute dwells at two major resonances
- No data loss occurs with 1 G 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3-minute dwells at two major resonances

5.8.1.3 Random vibration (Rotational)

The drive will meet the criteria shown below while operating in the specified conditions:

- Less than 20% Performance degradation for Random Write/Read/Verify @12.5Rad/sec^2('10-300Hz Flat)

5.8.2 Nonoperating vibration

The drive does not sustain permanent damage or loss of previously recorded data after being subjected to the environment described below

5.8.2.1 Random vibration

The test consists of a random vibration applied for each of three mutually perpendicular axes with the time duration of 10 minutes per axis. The PSD levels for the test simulate the shipping and relocation environment shown below. The overall RMS (Root Mean Square) level of vibration is 1.04 G.

Frequency	2 Hz	4 Hz	8 Hz	40 Hz	55 Hz	70 Hz	200 Hz
G2/Hz	0.001	0.03	0.03	0.003	0.01	0.01	0.001

Table 36 Random vibration PSD profile break points (nonoperating)

5.8.2.2 Swept sine vibration

- 2 G (Zero to peak), 5 to 500 to 5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwell at two major resonances

5.8.3 Operating shock

The drive meets the following criteria while operating in the conditions described below. The shock test consists of 10 shock inputs in each axis and direction for total of 60. There must be a delay between shock pulses long enough to allow the drive to complete all necessary error recovery procedures.

- No error occurs with a 10 G half-sine shock pulse of 11 ms duration in all models.
- No data loss occurs with a 30 G half-sine shock pulse of 4 ms duration in all models.
- No data loss occurs with a 70 G half-sine shock pulse of 2 ms duration.

5.8.4 Non-operating shock

The drive will operate with no degradation of performance after being subjected to shock pulses with the following characteristics.

5.8.4.1 Trapezoidal shock wave

- Approximate square (trapezoidal) pulse shape
- Approximate rise and fall time of pulse is1 ms
- Average acceleration level is 50 G. (Average response curve value during the time following the 1 ms rise time and before the 1 ms fall with a time “duration of 11 ms”)
- Minimum velocity change is 4.23 meters/second

5.8.4.2 Sinusoidal shock wave

The shape is approximately half-sine pulse. The figure below shows the maximum acceleration level and duration.

Models	Accleration level (G)	Duration (ms)
All models	350	2
All models	150	11

Table 37 Sinusoidal shock wave

5.8.5 Non-operating Rotational shock

All shock inputs shall be applied around the actuator pivot axis.

Duration	Rad/sec^2
1 ms	30,000
2 ms	20,000

Table 38 Rotational Shock

5.9 Acoustics

The upper limit criteria of the octave sound power levels are given in Bels relative to one picowatt and are shown in the following table. The sound power emission levels are measured in accordance with ISO 7779.

Mode	Typical / Max	
	1 disk model	2 disk model
Idle	2.5 (2.8) / 2.7	2.6 / 2.8
Operating	2.7 (3.1) / 3.1	2.8 / 3.0

(Deskstar only)

Table 39 Sound power levels

Mode definition:

Idle mode. The drive is powered on, disks spinning, track following, unit ready to receive and respond to interface commands.

Operating mode. Continuous random cylinder selection and seek operation of the actuator with a dwell time at each cylinder. The seek rate for the drive is to be calculated as shown below:

- Dwell time = 0.5 x 60/RPM
- Seek rate = 0.4 / (Average seek time + Dwell time)

5.10 Identification labels

The following labels are affixed to every drive shipped from the drive manufacturing location in accordance with the appropriate hard disk drive assembly drawing:

- A label containing the Hitachi logo, the Hitachi Global Storage Technologies part number, and the statement “Made by Hitachi Global Storage Technologies Inc.” or Hitachi Global Storage Technologies approved equivalent
- A label containing the drive model number, the manufacturing date code, the formatted capacity, the place of manufacture, UL/CSA/TUV/CE/C-Tick mark logos
- A bar code label containing the drive serial number
- A label containing the jumper pin description
- A user designed label per agreement

The above labels may be integrated with other labels.

5.11 Safety

5.11.1 UL and CSA standard conformity

The product is qualified per UL60950-1 : 2003 First Edition and CAN/CSA-C22.2 No.60950-1-03 First Edition, for use in Information Technology Equipment including Electric Business Equipment.

The UL recognition or the CSA certification is maintained for the product life.

The UL and C-UL recognition mark or the CSA monogram for CSA certification appear on the drive.

5.11.2 German Safety Mark

The product is approved by TUV on Test requirement: EN60950-1 : 2001 but the GS mark is not applicable to internal devices such as this product.

5.11.3 Flammability

The printed circuit boards used in this product are made of material with the UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with the UL recognized flammability rating of V-2 minimum basically.

5.11.4 Safe handling

The product is conditioned for safe handling in regards to sharp edges and corners.

5.11.5 Substance restriction requirements

The product complies with the Directive 2002/95/EC of the European Parliament on the restrictions of the use of the certain hazardous substances in electrical and electronic equipment (RoHS).

5.11.6 Secondary circuit protection

Spindle/VCM driver module includes 12 V over current protection circuit.

5.12 Electromagnetic compatibility

When installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, the drive meets the following worldwide EMC requirements:

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15. (A 6 dB buffer shall be maintained on the emission requirements).
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).Spectrum Management Agency (SMA) EMC requirements of Australia. The SMA has approved two forms of C-Tick Marking for Hitachi Global Storage Technologies.

5.12.1 CE Mark

The product is declared to be in conformity with requirements of the following EC directives under the sole responsibility of Hitachi Global Storage Technologies Japan Ltd:

Council Directive 2004/108/EC on the approximation of laws of the Member States relating to electromagnetic compatibility.

5.12.2 C-Tick Mark

The product complies with the following Australian EMC standard:

Limits and methods of measurement of radio disturbance characteristics of information technology, AS/NZS 3548 : 1995 Class B.

5.12.3 BSMI Mark

The product complies with the Taiwan EMC standard “Limits and methods of measurement of radio disturbance characteristics of information technology equipment, CNS 13438 Class B.”

5.12.4 MIC Mark

The product complies with the Korea EMC standard. The regulation for certification of information and communication equipment is based on “Telecommunications Basic Act” and “Radio Waves Act” Korea EMC requirement are based technically on CISPR22:1993-12 measurement standards and limits. MIC standards are likewise based on IEC standards.

Part 2. Interface Specification

6.0 General

6.1 Introduction

This specification describes the host interface of HxP7250xxGLA3y0.

The interface conforms to the following working documents of Information technology with certain limitations described in the section 6.3 “Deviations from Standard” on page 58

– Serial ATA II: Extensions to Serial ATA Revision 2.6

6.2 Terminology

Device	Device indicates HxP7250xxGLA3y0
Host	Host indicates the system that the device is attached to.

6.3 Deviations From Standard

The device conforms to the referenced specifications, with deviations described below.

Check Power Mode	Check Power Mode command returns FFh to Sector Count Register when the device is in Idle mode. This command does not support 80h as the return value.
COMRESET	COMRESET response is not the same as that of Power On Reset. Refer to section 5.1, “Reset Response” for detail.
Download	Download command is aborted when the device is in security locked mode.
COMRESET response time	During 500ms from Power On Reset, COMINIT is not returned within 10ms as a response to COMRESET.
Streaming Commands	When the device is in standby mode, Streaming Commands can’t be completed while waiting for the spindle to reach operating speed even if execution time exceeds specified CCTL(Command Completion Time Limit). The minimum CCTL is 50ms.CCTL is set to 50ms when the specified value is shorter than 50ms.
Error Recover Control (SCT Command set)	When the device is in standby mode, any command where error recovery time limit is specified can’t be completed while waiting for the spindle to reach operating speed even if execution time exceeds specified recovery time limit. The minimum time limit is 6.5 second. When the specified time limit is shorter than 6.5 second, the issued command is aborted.

7.0 Registers

In Serial ATA, the host adapter contains a set of registers that shadow the contents of the traditional device registers, referred to as the Shadow Register Block. Shadow Register Block registers are interface registers used for delivering commands to the device or posting status from the device. About details, please refer to the Serial ATA Specification.

In the following cases, the host adapter sets the BSY bit in its shadow Status Register and transmits a FIS to the device containing the new contents.

- Command register is written in the Shadow Register Block
- Device Control register is written in the Shadow Register Block with a change of state of the SRST bit
- COMRESET is requested

7.1 Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC /SERV	DRQ	COR	IDX	ERR

Table 40 Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See 7.13 "Status Register" on the page 62 for the definition of the bits in this register.

7.2 Command register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in 10.0 Command Descriptions on page 115.

All other registers required for the command must be set up before writing the Command Register.

7.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

The cylinder number may be from zero to the number of cylinders minus one.

When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 16-23, and the "previous content" contains Bits 40-47. The 48-bit Address feature set is described in 8.15.

7.4 Cylinder Low Register

This register contains the low order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

The cylinder number may be from zero to the number of cylinders minus one.

When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 8-15, and the "previous content" contains Bits 32-39.

7.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command, and configuration information is transferred on an Identify Device command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

7.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
HOB	-	-	-	1	SRST	-IEN	0

Table 41 Device Control Register

Bit Definitions

HOB

HOB (high order byte) is defined by the 48-bit Address feature set. A write to any Command Register shall clear the HOB bit to zero.

SRST (RST)

Software Reset. The device is held reset when RST=1. Setting RST=0 reenables the device.

The host must set RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the device recognizes the reset.

-IEN

Interrupt Enable. When -IEN=0, and the device is selected, device interrupts to the host will be enabled. When -IEN=1, or the device is not selected, device interrupts to the host will be disabled.

7.7 Drive Address Register

Drive Address Register							
7	6	5	4	3	2	1	0
HIZ	-WTG	-H3	-H2	-H1	-H0	-DS1	-DS0

Table 42 Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit Definitions

HIZ

High Impedance. This bit is not driven and will always be in a high impedance state.

-WTG

-Write Gate. This bit is 0 when writing to the disk device is in progress.

-H3,-H2,-H1,-H0 -Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. -H0 is the least significant.

-DS1 -Drive Select 1. Drive select bit for device 1, active low. DS1=0 when device 1 (slave) is selected and active.

-DS0 -Drive Select 0. Drive Select bit for device 0, active low. DS0=0 when device 0 (master) is selected and active.

7.8 Device/Head Register

Device/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Table 43 Device/Head Register

This register contains the device and head numbers.

Bit Definitions

L Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.

DRV Device. This product ignores this bit.

HS3,HS2,HS1,HS0 Head Select. These four bits indicate binary encoded address of the head. HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head.
The head number may be from zero to the number of heads minus one.
In LBA mode, HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

7.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
ICRCE	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Table 44 Error Register

This register contains status from the last command executed by the device, or a diagnostic code.

At the completion of any command except Execute Device Diagnostic, the contents of this register are valid always even if ERR=0 in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. See 0 on page 65 for the definition.

Bit Definitions

ICRCE (CRC) Interface CRC Error. ICRCE=1 indicates a CRC error occurred during FIS transmission or FIS reception.

UNC Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.

IDNF (IDN) ID Not Found. IDN=1 indicates the requested sector's ID field could not be found.

ABRT (ABT) Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register.

TK0NF (T0N) Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.

AMNF (AMN) Address Mark Not Found. This product does not report this error. This bit is always zero.

7.10 Features Register

This register is command specific. This is used with the Set Features command, SMART Function Set command and Format Unit command.

7.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors (in 28-bit addressing) or 65,536 sectors (in 48-bit addressing) is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

7.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.

When 48-bit commands are used, the "most recently written" content contains LBA Bits 0-7, and the "previous content" contains Bits 24-31.

7.13 Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC /SERV	DRQ	CORR	IDX	ERR

Table 45 Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit Definitions

BSY Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.

DRDY (RDY) Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to 0 during power on until the device is ready to accept a command. If the device detects an error while processing a command, RDY is set to 0 until the Status Register is read by the host, at which time RDY is set back to 1.

DF Device Fault. This product does not support DF bit. DF bit is always zero.

DSC Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to 0 by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status.

When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of not spinning up.

SERV (SRV) Service. This product does not support SERV bit.

DRQ Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.

CORR (COR) Corrected Data. Always 0.

IDX Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore, the host should not attempt to use IDX for timing purposes.

ERR Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets ERR=0 when the next command is received from the host.

8.0 General Operation Descriptions

8.1 Reset Response

There are three types of reset in ATA as follows:

Power On Reset (POR) The device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametric, and sets default values.

COMRESET COMRESET is issued in Serial ATA bus.
The device resets the interface circuitry as well as Soft Reset.

Soft Reset (Software Reset) SRST bit in the Device Control Register is set, and then is reset.
The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset are shown in Table 46.

	POR	COMRESET	Soft Reset
Aborting Host interface	-	o	o
Aborting Device operation	-	(*1)	(*1)
Initialization of hardware	o	x	x
Internal diagnostic	o	x	x
Spinning spindle	o	x	x
Initialization of registers (*2)	o	o	o
Reverting programmed parameters to default - Number of CHS (set by Initialize Device Parameter) - Multiple mode - Write cache - Read look-ahead - ECC bytes	o	(*3)	(*3)
Disable Standby timer	o	x	x
Power mode	(*5)	(*4)	(*4)

o ---- execute
x ---- not execute

Table 46 Reset Response.

Table Notes

(*1) Execute after the data in write cache has been written.

(*2) Default value on POR is shown in Table 47 Default Register Values on page 65.

(*3) The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

(*4) In the case of Sleep mode, the device goes to Standby mode. In other case, the device does not change current mode.

(*5) Idle when Power-Up in Standby feature set is disabled. Standby when Power-Up in Standby feature set is enabled.

8.1.1 Register Initialization

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	A0h
Status	50h
Alternate Status	50h

Table 47 Default Register Values

After power on, hard reset, or software reset, the register values are initialized as shown in Table 47.

Code	Description
01h	No error Detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error

Table 48 Diagnostic Codes

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Device Diagnostic command is shown in Table 48.

8.2 Diagnostic and Reset considerations

In each case of Power on Reset, COMRESET, Soft reset, and EXECUTE DEVICE DIAGNOSTIC command, the device is diagnosed. And Error register is set as shown in 0.

8.3 Sector Addressing Mode

All addressing of data sectors recorded on the device's media is by a logical sector address. The logical CHS address for HxP7250xxGLA3y0 is different from the actual physical CHS location of the data sector on the disk media. All addressing of data sectors recorded on the device's media.

HxP7250xxGLA3y0 support both Logical CHS Addressing Mode and LBA Addressing Mode as the sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. So a host system must set the L bit to 1 if the host uses LBA Addressing mode.

8.3.1 Logical CHS Addressing Mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but can not exceed 255(0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but can not exceed 15(0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535(0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode also is described in the Identify Device Information.

8.3.2 LBA Addressing Mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true:

```
LBA =( (cylinder * heads_per_cylinder + heads)
                * sectors_per_track ) + sector - 1
```

where heads_per_cylinder and sectors_per_track are the current translation mode values.

On LBA addressing mode, the LBA value is set to the following register.

Device/Head	<---	LBA bits	27-24
Cylinder High	<---	LBA bits	23-16
Cylinder Low	<---	LBA bits	15- 8
Sector Number	<---	LBA bits	7- 0

8.4 Power Management Feature

The power management feature set permits a host to modify the behavior in a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enables a device to implement low power consumption modes.

HxP7250xxGLA3y0 implement the following set of functions.

1. A Standby timer
2. Idle command
3. Idle Immediate command
4. Sleep command
5. Standby command
6. Standby Immediate command

8.4.1 Power Mode

The lowest power consumption when the device is powered on occurs in Sleep Mode. When in sleep mode, the device requires a reset to be activated.

In Standby Mode the device interface is capable of accepting commands, but as the media may not immediately accessible, there is a delay while waiting for the spindle to reach operating speed.

In Idle Mode the device is capable of responding immediately to media access requests.

In Active Mode the device is under executing a command or accessing the disk media with read look-ahead function or writes cache function.

8.4.2 Power Management Commands

The Check Power Mode command allows a host to determine if a device is currently in, going to or leaving standby mode.

The Idle and Idle Immediate commands move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.

The Standby and Standby Immediate commands move a device to standby mode immediately from the active or idle modes. The standby command also sets the standby timer count.

The Sleep command moves a device to sleep mode. The device's interface becomes inactive at the completion of the sleep command. A reset is required to move a device out of sleep mode. When a device exits sleep mode it will enter Standby mode.

8.4.3 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.

If the value of SECTOR COUNT register on Idle command or Standby command is set to 00h, the standby timer is disabled.

8.4.4 Interface Capability for Power Modes

Each power mode affects the physical interface as defined in the following table:

Mode		BSY	RDY	Interface active	Media
Active		x	x	Yes	Active
Idle		0	1	Yes	Active
Standby		0	1	Yes	Inactive
sleep		x	x	No	Inactive

Table 49 Power conditions

Ready (RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

8.5 SMART Function

The intent of Self-monitoring, analysis and reporting technology (SMART) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

8.5.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

8.5.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. The valid range of attribute values is from 1 to 253 decimal. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or faulty condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or faulty condition existing.

8.5.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical values of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

8.5.4 Threshold exceeded condition

If one or more attribute values, whose Pre-failure bit of their status flag is set, are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

8.5.5 SMART commands

The SMART commands provide access to attribute values, attribute thresholds and other logging and reporting information.

8.5.6 Off-line Read Scanning

The device provides the off-line read scanning feature with reallocation. This is the extension of the off-line data collection capability. The device performs the entire read scan with reallocation for the marginal sectors to prevent the user data lost.

If interrupted by the host during the read scanning, the device services the host command.

8.5.7 Error Log

Logging of reported errors is supported. The device provides information on the last five errors that the device reported as described in SMART error log sector. The device may also provide additional vendor specific information on these reported errors. The error log is not disabled when SMART is disabled. Disabling SMART shall disable the delivering of error log information via the SMART READ LOG SECTOR command.

If a device receives a firmware modification, all error log data is discarded and the device error count for the life of the device is reset to zero.

8.5.8 Self-test

The device provides the self-test features which are initiated by SMART Execute Off-line Immediate command. The self-test checks the fault of the device, reports the test status in Device Attributes Data and stores the test result in the SMART self-test log sector as described in SMART self-test log data structure. All SMART attributes are updated accordingly during the execution of self-test.

If interrupted by the host during the self-tests, the device services the host command.

If the device receives a firmware modification, all self-test log data is discarded.

8.6 Security Mode Feature Set

Security Mode Feature Set is a powerful security feature. With a device lock password, a user can prevent unauthorized access to hard disk device even if the device is removed from the computer.

The following commands are supported for this feature.

Security Set Password	('F1'h)
Security Unlock	('F2'h)
Security Erase Prepare	('F3'h)
Security Erase Unit	('F4'h)
Security Freeze Lock	('F5'h)
Security Disable Password	('F6'h)

8.6.1 Security mode

Following security modes are provided.

Device Locked mode The device disables media access commands after power on. Media access commands are enabled by either a security unlock command or a security erase unit command.

Device Unlocked mode The device enables all commands. If a password is not set this mode is entered after power on, otherwise it is entered by a security unlock or a security erase unit command.

Device Frozen mode The device enables all commands except those which can update the device lock function, set/change password. The device enters this mode via a Security Freeze Lock command. It cannot quit this mode until power off.

8.6.2 Security Level

Following security levels are provided.

High level security When the device lock function is enabled and the User Password is forgotten the device can be unlocked via a Master Password.

Maximum level security When the device lock function is enabled and the User Password is forgotten then only the Master Password with a Security Erase Unit command can unlock the device. Then user data is erased.

8.6.3 Password

This function can have 2 types of passwords as described below.

Master Password When the Master Password is set, the device does NOT enable the Device Lock Function, and the device can NOT be locked with the Master Password, but the Master Password can be used for unlocking the device locked.

Identify Device Information word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 0001h through FFFEh.

User Password The User Password should be given or changed by a system user. When the User Password is set, the device enables the Device Lock Function, and then the device is locked on next power on reset or hard reset.

The system manufacturer/dealer who intends to enable the device lock function for the end users, must set the master password even if only single level password protection is required.

8.6.4 Operation example

8.6.4.1 Master Password setting

The system manufacturer/dealer can set a new Master Password from default Master Password using the Security Set Password command, without enabling the Device Lock Function.

The Master Password Revision Code is set to FFFEh as shipping default by the HDD manufacturer

8.6.4.2 User Password setting

When a User Password is set, the device will automatically enter lock mode the next time the device is powered on.

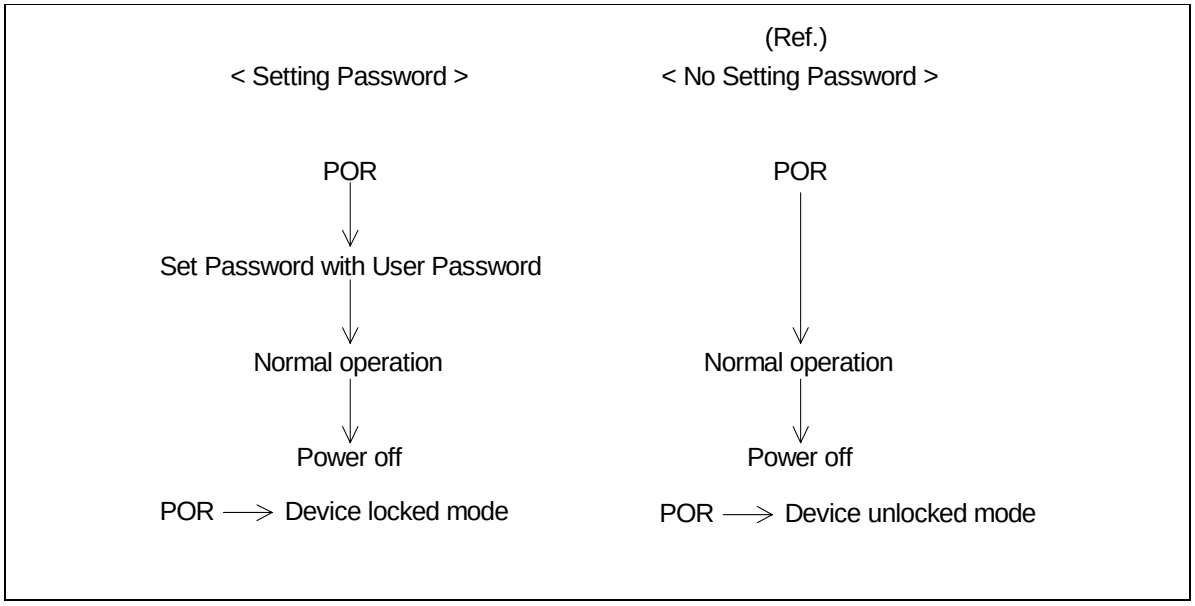
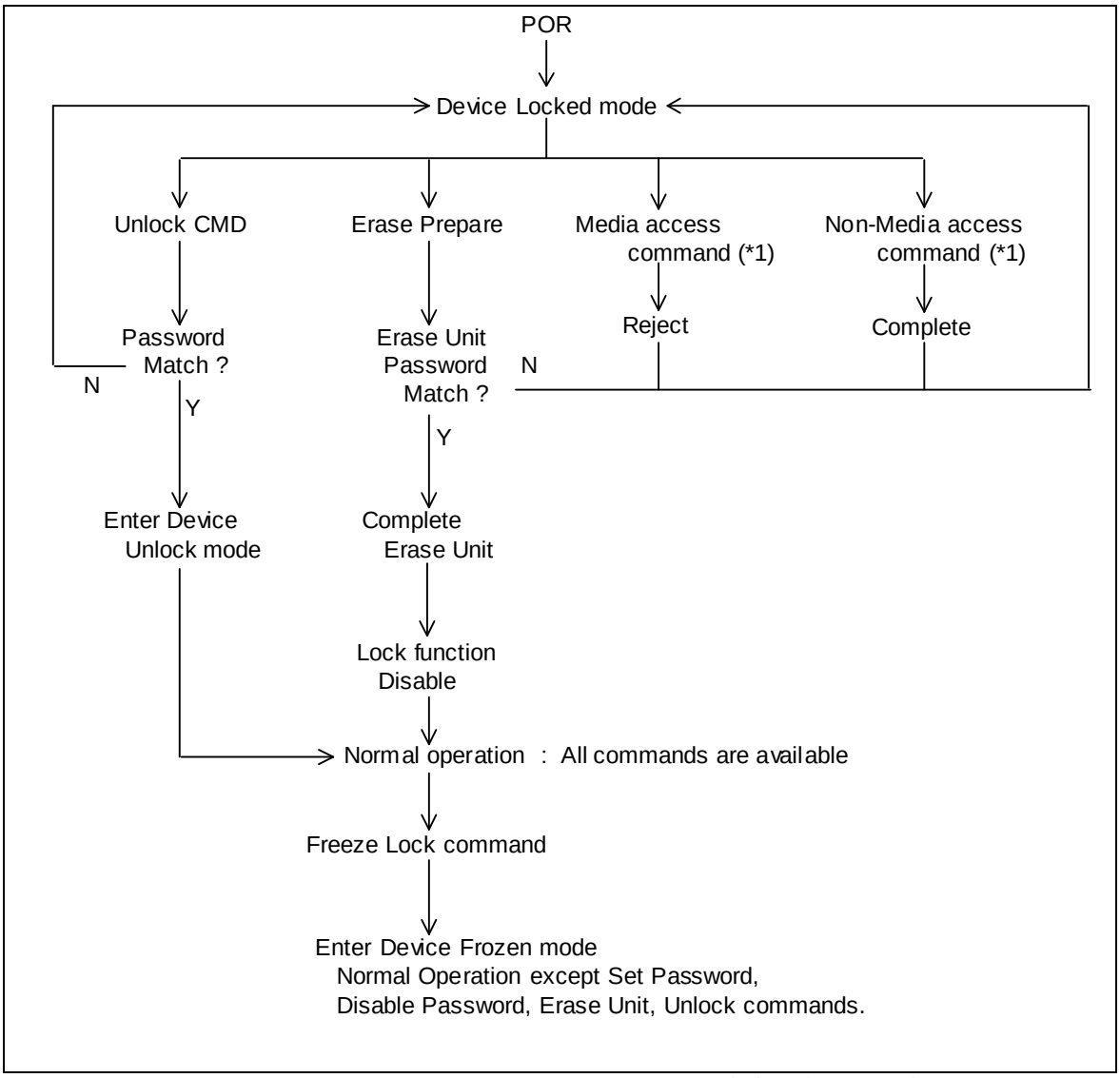


Figure 28 Initial Setting

8.6.4.3 Operation from POR after User Password is set

When Device Lock Function is enabled, the device rejects media access command until a Security Unlock command is successfully completed.



(*1) Refer to Section 8.6.5 on page 74

Figure 29 Usual Operation

8.6.4.4 User Password Lost

If the User Password is forgotten and High level security is set, the system user can't access any data. However, the device can be unlocked using the Master Password.

If a system user forgets the User Password and Maximum security level is set, data access is impossible. However, the device can be unlocked using the Security Erase Unit command to unlock the device and erase all user data with the Master Password.

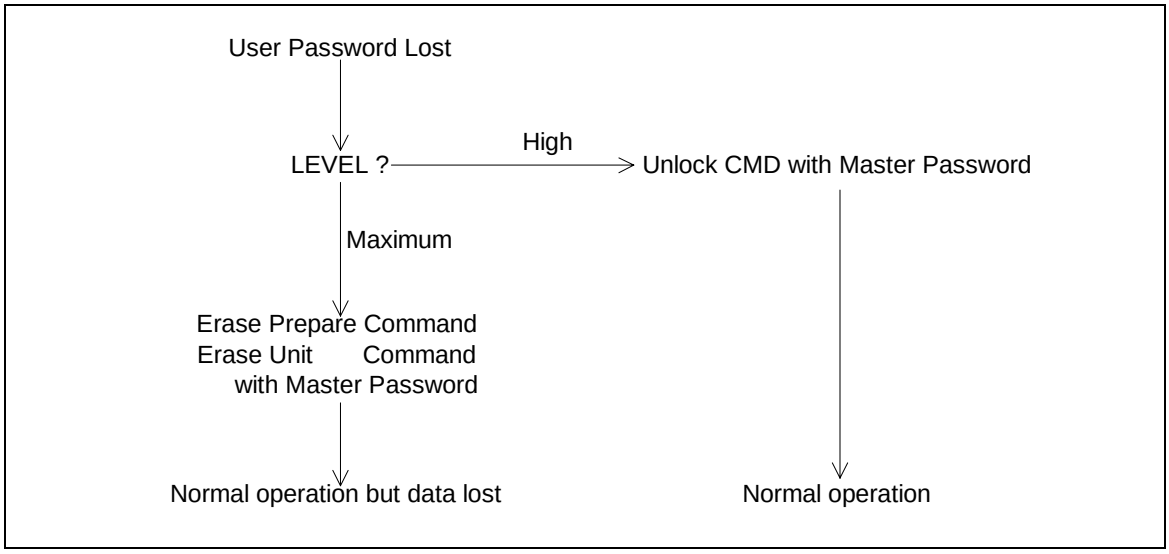


Figure 30 Password Lost

8.6.4.5 Attempt limit for SECURITY UNLOCK command

The SECURITY UNLOCK command has an attempt limit. The purpose of this attempt limit is to prevent that someone attempts to unlock the drive by using various passwords many times.

The device counts the password mismatch. If the password does not match, the device counts it up without distinguishing the Master password and the User password. If the count reaches 5, EXPIRE bit (bit 4) of Word 128 in Identify Device information is set, and then SECURITY ERASE UNIT command and SECURITY UNLOCK command are aborted until a hard reset or a power off. The count and EXPIRE bit are cleared after a power on reset or a hard reset.

8.6.5 Command Table

This table shows the device's response to commands when the Security Mode Feature Set (Device lock function) is enabled.

Command	Locked Mode	Unlocked Mode	Frozen Mode
Check Power Mode	Executable	Executable	Executable
Configure Stream	Command aborted	Executable	Executable
Execute Device Diagnostic	Executable	Executable	Executable
Device Configuration Restore	Command aborted	Executable	Executable
Device Configuration Freeze Lock	Command aborted	Executable	Executable
Device Configuration Identify	Command aborted	Executable	Executable
Device Configuration Set	Command aborted	Executable	Executable
Download Microcode	Command aborted	Executable	Executable
Flush Cache	Command aborted	Executable	Executable
Flush Cache Ext	Command aborted	Executable	Executable
Format Track	Command aborted	Executable	Executable
Identify Device	Executable	Executable	Executable
Idle	Executable	Executable	Executable
Idle Immediate	Executable	Executable	Executable
Initialize Device Parameters	Executable	Executable	Executable
Read Buffer	Executable	Executable	Executable
Read DMA	Command aborted	Executable	Executable
Read DMA Ext	Command aborted	Executable	Executable
Read FPDMA Queued	Command aborted	Executable	Executable
Read Log Ext	Executable	Executable	Executable
Read Multiple	Command aborted	Executable	Executable
Read Multiple Ext	Command aborted	Executable	Executable
Read Native Max Address	Executable	Executable	Executable
Read Native Max Ext	Executable	Executable	Executable
Read Sector(s)	Command aborted	Executable	Executable
Read Sector(s) Ext	Command aborted	Executable	Executable
Read Stream DMA	Command aborted	Executable	Executable
Read Stream PIO	Command aborted	Executable	Executable
Read Verify Sector(s)	Command aborted	Executable	Executable
Read Verify Sector(s) Ext	Command aborted	Executable	Executable
Recalibrate	Executable	Executable	Executable
SCT Read/Write Long	Command aborted	Command aborted	Command aborted
SCT Write Same	Command aborted	Executable	Executable
SCT Error Recovery Control	Command aborted	Executable	Executable
SCT Feature Control	Command aborted	Executable	Executable
SCT Data Table	Command aborted	Executable	Executable
SCT Read Status	Executable	Executable	Executable
Security Disable Password	Command aborted	Executable	Command aborted
Security Erase Prepare	Executable	Executable	Command aborted

Table 50 Command table for device lock operation - 1

Command	Locked Mode	Unlocked Mode	Frozen Mode
Security Erase Unit	Executable	Executable	Command aborted
Security Freeze Lock	Command aborted	Executable	Executable
Security Set Password	Command aborted	Executable	Command aborted
Security Unlock	Executable	Executable	Command aborted
Seek	Executable	Executable	Executable
Set Features	Executable	Executable	Executable
Set Max Address	Command aborted	Executable	Executable
Set Max Address Ext	Command aborted	Executable	Executable
Set Multiple Mode	Executable	Executable	Executable
Sleep	Executable	Executable	Executable
SMART Disable Operations	Executable	Executable	Executable
SMART Enable/Disable Attributes Autosave	Executable	Executable	Executable
SMART Enable Operations	Executable	Executable	Executable
SMART Execute Off-line Immediate	Executable	Executable	Executable
SMART Read Attribute Values	Executable	Executable	Executable
SMART Read Attribute Thresholds	Executable	Executable	Executable
SMART Return Status	Executable	Executable	Executable
SMART Save Attribute Values	Executable	Executable	Executable
SMART Read Log Sector	Executable	Executable	Executable
SMART Write Log Sector	Executable	Executable	Executable
SMART Enable/Disable Automatic Off-Line	Executable	Executable	Executable
Standby	Executable	Executable	Executable
Standby Immediate	Executable	Executable	Executable
Write Buffer	Executable	Executable	Executable
Write DMA	Command aborted	Executable	Executable
Write DMA Ext	Command aborted	Executable	Executable
Write DMA FUA Ext	Command aborted	Executable	Executable
Write FPDMA Queued	Command aborted	Executable	Executable
Write Log Ext	Command aborted	Executable	Executable
Write Multiple	Command aborted	Executable	Executable
Write Multiple Ext	Command aborted	Executable	Executable
Write Multiple FUA Ext	Command aborted	Executable	Executable
Write Sector(s)	Command aborted	Executable	Executable
Write Sector(s) Ext	Command aborted	Executable	Executable
Write Stream DMA	Command aborted	Executable	Executable
Write Stream PIO	Command aborted	Executable	Executable
Write Uncorrectable Ext	Command aborted	Executable	Executable

Table 51 Command table for device lock operation - 2

8.7 Host Protected Area Feature

Host Protected Area Feature is to provide the 'protected area' which can not be accessed via conventional method. This 'protected area' is used to contain critical system data such as BIOS or system management information. The contents of entire system main memory may also be dumped into 'protected area' to resume after system power off.

The LBA/CYL changed by following command affects the Identify Device Information.

The following set of commands is implemented for this function.

Read Native Max ADDRESS	('F8'h)
Set Max ADDRESS	('F9'h)

8.7.1 Example for operation (In LBA mode)

Assumptions:

For better understanding, the following example uses actual values for LBA, size, etc. Since it is just an example, these values could be different.

Device characteristics

Capacity (native)	:	6,498,680,832	byte (6.4GB)
Max LBA (native)	:	12,692,735	(0FFFFFh)
Required size for protected area	:	206,438,400	byte
Required blocks for protected area	:	403,200	(062700h)
Customer usable device size	:	6,292,242,432	byte (6.2GB)
Customer usable sector count	:	12,289,536	(BB8600h)
LBA range for protected area	:	BB8600h to C1ACFFh	

1. Shipping HDDs from HDD manufacturer

When the HDDs are shipped from HDD manufacturer, the device has been tested to have usable capacity of 6.4GB besides flagged media defects not to be visible by system.

2. Preparing HDDs at system manufacturer

Special utility software is required to define the size of protected area and store the data into it.
The sequence is:

Issue Read Native Max Address command to get the real device maximum LBA. Returned value shows that native device Maximum LBA is 12,692,735 (C1ACFFh) regardless of the current setting.

Make entire device be accessible including the protected area by setting device Maximum LBA as 12,692,735 (C1ACFFh) via Set Max Address command. The option could be either nonvolatile or volatile.

Test the sectors for protected area (LBA >= 12,289,536 (BB8600h)) if required.

Write information data such as BIOS code within the protected area.

Change maximum LBA using Set Max Address command to 12,289,535 (BB85FFh) with nonvolatile option.

From this point, the protected area cannot be accessed till next Set Max Address command is issued. Any BIOSes, device drivers, or application software access the HDD as if that is the 6.2GB device because the device acts exactly the same as real 6.2GB device does.

3. Conventional usage without system software support

Since the HDD works as 6.2GB device, there is no special care to use this device for normal use.

4. Advanced usage using protected area

The data in the protected area is accessed by following.

Issue Read Native Max Address command to get the real device maximum LBA. Returned value shows that native device Maximum LBA is 12,692,735 (C1ACFFh) regardless of the current setting.

Make entire device be accessible including the protected area by setting device Maximum LBA as 12,692,735 (C1ACFFh) via Set Max Address command with volatile option. By using this option, unexpected power removal or reset will not make the protected area remained accessible.

Read information data from protected area.

Issue hard reset or POR to inhibit any access to the protected area.

8.7.2 Security extensions

1. Set Max Set Password
2. Set Max Lock
3. Set Max Freeze Lock
4. Set Max Unlock.

The Set Max Set Password command allows the host to define the password to be used during the current power on cycle. The password does not persist over a power cycle but does persist over a hardware or software reset. This password is not related to the password used for the Security Mode Feature set. When the password is set the device is in the Set_Max_Unlocked mode. The Set Max Lock command allows the host to disable the Set Max commands (except set Max Unlock) until the next power cycle or the issuance and acceptance of the Set Max Unlock command. When this command is accepted the device is in the Set_Max_Locked mode. The Set Max Unlock command changes the device from the Set_Max_Locked mode to the Set_Max_Unlocked mode. The Set Max Freeze Lock command allows the host to disable the Set Max commands (including Set Max UNLOCK) until the next power cycle. When this command is accepted the device is in the Set_Max_Frozen mode.

The IDENTIFY DEVICE response word 83, bit 8 indicates that this extension is supported if set, and word 86, bit 8 indicate the Set Max security extension enabled if set.

8.8 Seek Overlap

HxP7250xxGLA3y0 provide accurate seek time measurement method. The seek command is usually used to measure the device seek time by accumulating execution time for a number of seek commands. With typical implementation of the seek command, this measurement must including the device and host command overhead. To eliminate this overhead, HxP7250xxGLA3y0 overlaps the seek command as described below.

The first seek command completes before the actual seek operation is end. Then device can receive the next seek command from the host but actual seek operation for the next seek command starts right after the actual seek operation for the first seek command is completed. In other words, the executions of two seek commands overlaps excluding the actual seek operation.

With this overlap, total elapsed time for a number of seek commands results the total accumulated time for actual seek operation plus one pre and post overhead. When the number of seeks is large, this just one overhead can be ignored.

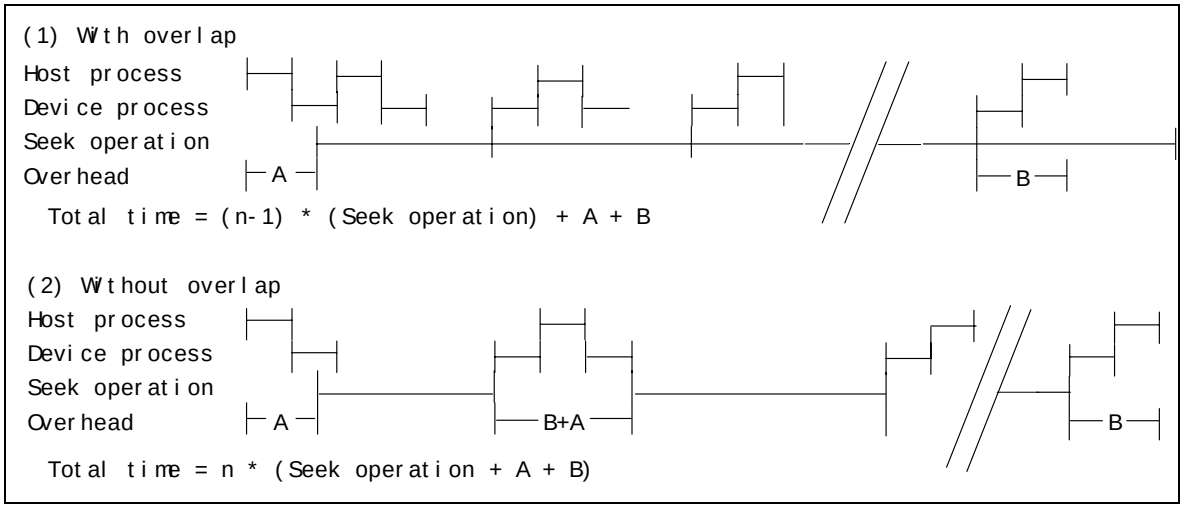


Figure 31 Seek overlap

8.9 Write Cache Function

Write cache is a performance enhancement whereby the device reports as completing the write command (Write Sector(s), Write Multiple and Write DMA) to the host as soon as the device has received all of the data into its buffer. And the device assumes responsibility to write the data subsequently onto the disk.

- While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation. But power off terminates writing operation immediately and unwritten data are to be lost.
- Soft reset, Standby (Immediate) command and Flush Cache commands during writing the cached data are executed after the completion of writing to media. So the host system can confirm the completion of write cache operation by issuing Soft reset, Standby (Immediate) command or Flush Cache command to the device before power off.

8.10 Reassign Function

The reassign Function is used with read commands and write commands. The sectors of data for reassignment are prepared as the spare data sector.

This reassignment information is registered internally, and the information is available right after completing the reassign function. Also the information is used on the next power on reset or hard reset.

If the number of the spare sector reaches 0 sectors, the reassign function will be disabled automatically.

The spare tracks for reassignment are located at regular intervals from Cylinder 0. As a result of reassignment, the physical location of logically sequenced sectors will be dispersed.

8.10.1 Auto Reassign Function

The sectors those show some errors may be reallocated automatically when specific conditions are met. The spare tracks for reallocation are located at regular intervals from Cylinder 0. The conditions for auto-reallocation are described below.

Non recovered write errors

When a write operation can not be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation is failed.

If the write cache function is ENABLED, and when the number of available spare sectors reaches 0 sectors, both auto reassign function and write cache function are disabled automatically.

Non recovered read errors

When a read operation is failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

Recovered read errors

When a read operation for a sector failed once then recovered at the specific ERP step, this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the pre-defined conditions.

8.11 Power-up in Standby feature set

Power-Up In Standby feature set allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.

This feature set will be enabled/disabled via the SET FEATURES command or use of jumper. When enabled by a jumper, the feature set shall not be disabled via the SET FEATURES command. The enabling of this feature set shall be persistent after power cycle.

A device needs a SET FEATURES subcommand to spin-up to active state when the device has powered-up into Standby. The device remains in Standby until the SET FEATURES subcommand is received.

If power-up into Standby is enabled, when an IDENTIFY DEVICE is received while the device is in Standby as a result of powering up into Standby, the device shall set word 0 bit 2 to one to indicate that the response is incomplete, then only words 0 and 2 are correctly reported.

The IDENTIFY DEVICE information indicates the states as follows:

- identify device information is complete or incomplete
- this feature set is implemented
- this feature set is enabled or disabled
- the device needs the Set Features command to spin-up into active state

8.12 Advanced Power Management feature set (APM)

This feature allows the host to select an advanced power management level. The advanced power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing advanced power management levels. Device power consumption may increase with increasing advanced power management levels. The advanced power management levels contain discrete bands, described in the section of Set Feature command in detail. This feature set uses the following functions:

1. A SET FEATURES subcommand to enable Advanced Power Management
2. A SET FEATURES subcommand to disable Advanced Power Management

Advanced Power Management is independent of the Standby timer setting. If both Advanced Power Management and the Standby timer are set, the device will go to the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that the Standby state should be entered.

The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management feature is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set. Word 91, bits 7-0 contain the current Advanced Power Management level if Advanced Power Management is enabled.

8.13 Automatic Acoustic Management feature set (AAM)

This feature set allows the host to select an acoustic management level. The acoustic management level ranges the setting of 80h to FEh. Device performance and acoustic emanation may increase with increasing acoustic management levels. The acoustic management levels contain discrete bands, described in the section of the Set Feature command in detail.

The Automatic Acoustic Management feature set uses the following functions:

1. A SET FEATURES subcommand to enable Automatic Acoustic Management
2. A SET FEATURES subcommand to disable Automatic Acoustic Management

The IDENTIFY DEVICE response word 83, bit 9 indicates that Automatic Acoustic Management feature is supported if set. Word 86, bit 9 indicates that Automatic Acoustic Management is enabled if set. Word 94, bits 7-0 contain the current Automatic Acoustic Management level if Automatic Acoustic Management is enabled, and bits 8-15 contain the Vendor's recommended AAM level.

8.14 Address Offset Feature

Computer systems perform initial code loading (booting) by reading from a predefined address on a disk drive. To allow an alternate bootable operating system to exist in a system reserved area on a disk drive this feature provides a Set Features function to temporarily offset the drive address space. The offset address space wraps around so that the entire disk drive address space remains addressable in offset mode. Max LBA in offset mode is set to the end of the system reserved area to protect the data in the user area when operating in offset mode. The Max LBA can be changed by an Set Max Address command, but any commands which access sectors across the original native maximum LBA are rejected with error, even if this protection is removed by an Set Max Address command.

Set Features subcommand code 09h Enable Address Offset Mode offsets address Cylinder 0, Head 0, Sector 1, and LBA 0, to the start of the non-volatile protected area established using the Set Max Address command. The offset condition is cleared by Subcommand 89h Disable Address Offset Mode, Hardware reset or Power on Reset. If Reverting to Power on Defaults has been enabled by Set Features command, it is cleared by Soft reset as well. Upon entering offset mode the capacity of the drive returned in the Identify Device data is the size of the former protected area. A subsequent Set Max Address command with the address returned by Read Max Address command allows access to the entire drive. Addresses wrap so the entire drive remains addressable.

If a non-volatile protected area has not been established before the device receives a Set Features Enable Address Offset Mode command, the command fails with Abort error status.

Disable Address Offset Feature removes the address offset and sets the size of the drive reported by the Identify Device command back to the size specified in the last non-volatile Set Max Address command.

8.14.1 Enable/Disable Address Offset Mode

Set Features subcommand code 09h Enable Address Offset Mode offsets address Cylinder 0, Head 0, Sector 1, and LBA 0, to the start of the non-volatile protected area established using the Set Max Address command. The offset condition is cleared by Subcommand 89h Disable Address Offset Mode, Hardware reset or Power on Reset. If Reverting to Power on Defaults has been enabled by Set Features command, it is cleared by Soft reset as well. Upon entering offset mode the capacity of the drive returned in the Identify Device data is the size of the former protected area. A subsequent Set Max Address command with the address returned by Read Max Address command allows access to the entire drive. Addresses wrap so the entire drive remains addressable.

If a non-volatile protected area has not been established before the device receives a Set Features Enable Address Offset Mode command, the command fails with Abort error status.

Disable Address Offset Feature removes the address offset and sets the size of the drive reported by the Identify Device command back to the size specified in the last non-volatile Set Max Address command.

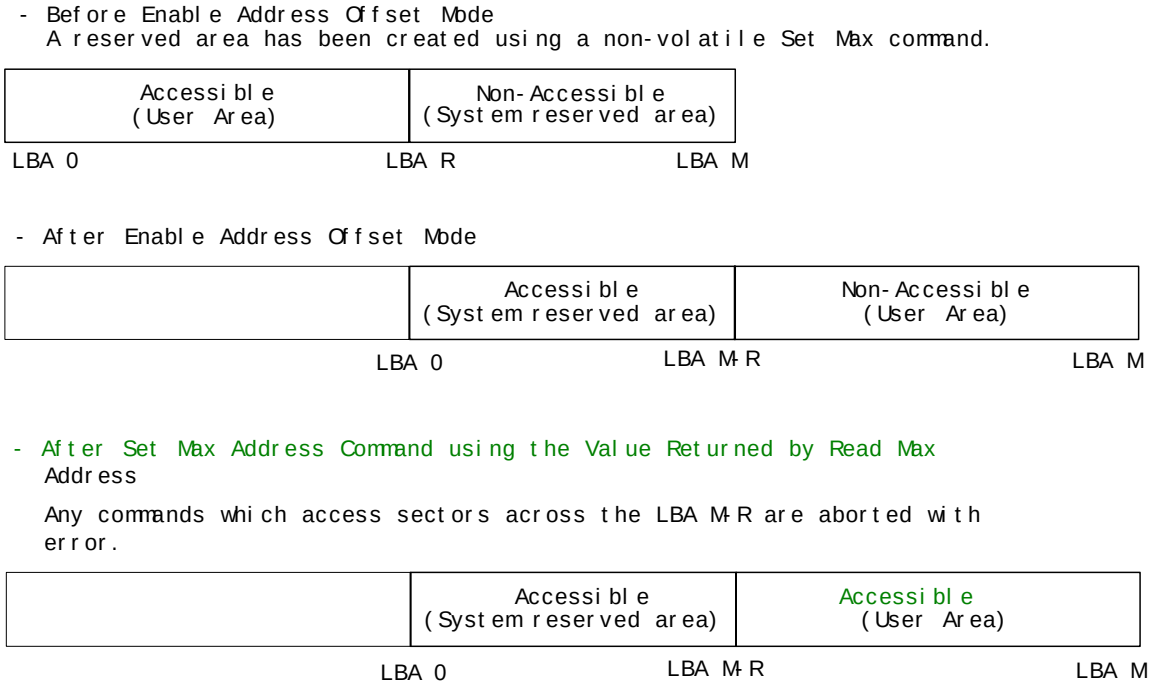


Figure 32 Device address map before and after Set Feature

8.14.2 Identify Device Data

Identify Device data word 83 bit 7 indicates the device supports the Address Offset Feature.

Identify Device data word 86 bit 7 indicates the device is in Address Offset mode.

8.14.3 Exceptions in Address Offset Mode

Any commands which access sectors across the original native maximum LBA are rejected with error, even if the access protection is removed by a Set Max Address command. If the sectors for Read Look Ahead operation include the original native maximum LBA, Read Look Ahead operation is not carried out even if it is enabled by Set Feature command.

8.15 48-bit Address Feature Set

The 48-bit Address feature set allows devices with capacities up to 281,474,976,710,655 sectors. This allows device capacity up to 144,115,188,075,855,360 bytes. In addition, the number of sectors that may be transferred by a single command are increased by increasing the allowable sector count to 16 bits.

Commands unique to the 48-bit Address feature set are:

- Flush Cache Ext
- Read DMA Ext
- Read FPDMA Queued
- Read Multiple Ext
- Read Native Max Address Ext
- Read Sector(s) Ext
- Read Verify Sector(s) Ext
- Set Max Address Ext
- Write DMA Ext
- Write DMA FUA Ext
- Write FPDMA Queued
- Write Multiple Ext
- Write Multiple FUA Ext
- Write Sector(s) Ext
- Write Uncorrectable Ext

The 48-bit Address feature set operates in LBA addressing only. Devices also implement commands using 28-bit addressing, and 28-bit and 48-bit commands may be intermixed.

In a device, the Features, the Sector Count, the Sector Number, the Cylinder High, and the Cylinder Low registers are a two-byte-deep FIFO. Each time one of these registers is written, the new content written is placed into the "most recently written" location and the previous content is moved to "previous content" location.

The host may read the "previous content" of the Features, the Sector Count, the Sector Number, the Cylinder High, and the Cylinder Low registers by first setting the High Order Bit (HOB, bit 7) of the Device control register to one and then reading the desired register. If HOB in the Device Control register is cleared to zero, the host reads the "most recently written" content when the register is read. A write to any Command Block register shall cause the device to clear the HOB bit to zero in the Device Control register. The "most recently written" content always gets written by a register write regardless of the state of HOB in the Device Control register.

Support of the 48-bit Address feature set is indicated in the Identify Device response bit 10 word 83. In addition, the maximum user LBA address accessible by 48-bit addressable commands is contained in Identify Device response words 100 through 103.

When the 48-bit Address feature set is implemented, the native maximum address is the value returned by a Read Native Max Address Ext command. If the native maximum address is equal to or less than 268,435,455, a Read Native Max Address shall return the native maximum address. If the native maximum address is greater than 268,435,455, a Read Native Max Address shall return a value of 268,435,455.

8.16 Streaming feature Set

The Streaming feature set is an optional feature set that allows a host to request delivery of data from a contiguous logical block address range within an allotted time. This places a priority on time to access the data rather than the integrity of the data. Streaming feature set commands only support 48-bit addressing.

A device that implements the Streaming feature set shall implement the following minimum set of commands:

- Configure Stream
- Read Stream PIO
- Write Stream PIO
- Read Stream DMA
- Write Stream DMA
- Read Log Ext

Support of the Streaming feature set is indicated in Identify Device work 84 bit 4.

Note that PIO versions of these commands limit the transfer rate (16.6 MB/s), provide no CRC protection, and limit status reporting as compared to a DMA implementation.

8.16.1 Streaming commands

The streaming commands are defined to be time critical data transfers rather than the standard data integrity critical commands. Each command shall be completed within the time specified in the Configure Stream command or in the streaming command itself in order to ensure the stream requirements of the AV type application. The device may execute background tasks as long as the Read Stream and Write Stream command execution time limits are still met.

Using the Configure Stream command, the host may define the various stream properties including the default Command Completion Time Limit (CCTL) to assist the device in setting up its caching for best performance. If the host does not use a Configure Stream command, the device shall use the CCTL specified in each streaming command, and the time limit is effective for one time only. If the CCTL is not set by Configure Stream command, the operation of a streaming command with a zero CCTL is device vendor specific. If Stream ID is not set by a Configure Stream command, the device shall operate according to the Stream ID set by the streaming command. The operation is device vendor specific.

The streaming commands may access any user LBA on a device. These commands may be interspersed with non-streaming commands, but there may be an impact on performance due to the unknown time required to complete the non-streaming commands.

The streaming commands should be issued using a specified minimum number of sectors transferred per command, as specified in word 95 of the Identify Device response. The transfer length of a request should be a multiple of the minimum number of sectors per transfer.

The host provided numeric stream identifier, Stream ID, may be used by the device to configure its resources to support the streaming requirements of the AV content. One Stream ID may be configured for each read and write operation with different command completion time limits be each Configure Stream command.

8.16.1.1 Urgent bit

The Urgent bit in the Read Stream and Write Stream commands specifies that the command should be completed in the minimum possible time by the device and shall be completed within the specified Command Completion Time Limit.

8.16.1.2 Flush to Disk bit

The Flush to Disk bit in the Write Stream command specifies that all data for the specified stream shall be flushed to the media before posting command completion. If a host requests flushes at times other than the end of each Allocation Unit, streaming performance may be degraded. The Set Features command to enable/disable caching shall not affect caching for streaming commands.

8.16.1.3 Not Sequential bit

The Not Sequential bit specifies that the next read stream command with the same Stream ID may not be sequential in LBA space. This information helps the device with pre-fetching decisions.

8.16.1.4 Read Continuous bit

If the Read Continuous bit is set to one for the command, the device shall transfer the requested amount of data to the host within the Command Completion Time Limit even if an error occurs. The data sent to the host by the device in an error condition is vendor specific.

8.16.1.5 Write Continuous bit

If the Write Continuous bit is set to one for the command, and an error is encountered, the device shall complete the request without posting an error. If an error cannot be resolved within the Command Completion Time Limit, the erroneous section on the media may be unchanged or may contain undefined data. A future read of this area may not report an error, even though the data is erroneous.

8.16.1.6 Handle Streaming Error bit

The Handle Streaming Error bit specifies to the device that this command starts at the LBA of a recently reported error section, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier. This mechanism allows the host to schedule error recovery and defect management for content critical data.

8.16.2 Streaming Logs

The Streaming Data Transfer feature set requires two error logs and one performance log. These logs are accessed via the Read Log Ext command; the information included in the error logs is volatile and is not maintained across power cycles, hard resets, or sleep. These error logs are 512 bytes in length and retain the last 31 errors that occurred during any Streaming Data transfer.

8.17 SATA BIST (Built-in Self Test)

The device supports the following BIST modes, and begins operations when it receives BIST Activate FIS.

F – Far End Analog Loopback.

L – Far End Retimed Loopback

T – Far End Transmit only

A – ALIGN Bypass (valid only in combination with T bit)

S – Bypass Scrambling (valid only in combination with T bit)

8.18 SATA Interface Power Management

The device supports both receiving host-initiated interface power management requests and initiating interface power management. The device initiates interface power management when the device enters its power saving mode whose power consumption is lower than Normal Idle mode.

8.19 Software Setting Preservation

When a device is enumerated, software will configure the device using SET FEATURES and other commands. These software settings are often preserved across software reset but not necessarily across hardware reset. In Parallel ATA, only commanded hardware resets can occur, thus legacy software only reprograms settings that are cleared for the particular type of reset it has issued. In Serial ATA, COMRESET is equivalent to hard reset and a non-commanded COMRESET may occur if there is an asynchronous loss of signal. Since COMRESET is equivalent to hardware reset, in the case of an asynchronous loss of signal some software settings may be lost without legacy software knowledge. In order to avoid losing important software settings without legacy driver knowledge, the software settings preservation ensures that the value of important software settings is maintained across a COMRESET. Software settings preservation may be enabled or disabled using SET FEATURES with a subcommand code of 06h. If a device supports software settings preservation, the feature shall be enabled by default.

8.19.1 COMRESET Preservation Requirements

The software settings that shall be preserved across COMRESET are listed below. The device is only required to preserve the indicated software setting if it supports the particular feature/command the setting is associated with.

INITIALIZE DEVICE PARAMETERS: Device settings established with the INITIALIZE DEVICE PARAMETERS command.

Power Management Feature Set Standby Timer: The Standby timer used in the Power Management feature set.

Read/Write Stream Error Log: The Read Stream Error Log and Write Stream Error Logs (accessed using READ LOG EXT and WRITE LOG EXT).

Security mode state: The security mode state established by Security Mode feature set commands (refer to section 6.13 of the ATA/6 specification). The device shall not transition to a different security mode state based on a COMRESET. For example, the device shall not transition from the SEC5: Unlocked / not Frozen state to state SEC4: Security enabled / Locked when a COMRESET occurs, instead the device shall remain in the SEC5: Unlocked / not Frozen state.

SECURITY FREEZE LOCK: The Frozen mode setting established by the SECURITY FREEZE LOCK command.

SECURITY UNLOCK: The unlock counter that is decremented as part of a failed SECURITY UNLOCK command attempt.

SET ADDRESS MAX (EXT): The maximum LBA specified in SET ADDRESS MAX or SET ADDRESS MAX EXT.

SET FEATURES (Write Cache Enable/Disable): The write cache enable/disable setting established by the SET FEATURES command with subcommand code of 02h or 82h.

SET FEATURES (Set Transfer Mode): PIO, Multiword, and UDMA transfer mode settings established by the SET FEATURES command with subcommand code of 03h.

SET FEATURES (Advanced Power Management Enable/Disable): The advanced power management enable/disable setting established by the SET FEATURES command with subcommand code of 05h or 85h. The advanced power management level established in the Sector Count register when advanced power management is enabled (SET FEATURES subcommand code 05h) shall also be preserved.

SET FEATURES (Read Look-Ahead): The read look-ahead enable/disable setting established by the SET FEATURES command with subcommand code of 55h or AAh.

SET FEATURES (Reverting to Defaults): The reverting to power-on defaults enable/disable setting established by the SET FEATURES command with a subcommand code of CCh or 66h.

SET MULTIPLE MODE: The block size established with the SET MULTIPLE MODE command.

8.20 SATA II Optional Features

There are several optional features defined in SATA II. The following shows whether these features are supported or not.

8.20.1 Asynchronous Signal Recovery

The device supports asynchronous signal recovery defined in SATA II.

8.20.2 Device Power Connector Pin 11 Definition

SATA II specification defines that Pin 11 of the power segment of the device connector may be used to provide the host with an activity indication and disabling of staggered spin-up. The device does not support both usage of Pin 11.

8.20.3 Phy Event Counters

Phy Event Counters are an optional feature to obtain more information about Phy level events that occur on the interface. This information may aid designers and integrators in testing and evaluating the quality of the interface. A device indicates whether it supports the Phy event counters feature in IDENTIFY (PACKET) DEVICE Word 76, bit 10. The host determines the current values of Phy event counters by issuing the READ LOG EXT command with a log page of 11h. The counter values shall not be retained across power cycles. The counter values shall be preserved across COMRESET and software resets.

The counters defined can be grouped into three basic categories: those that count events that occur during Data FIS transfers, those that count events that occur during non-Data FIS transfers, and events that are unrelated to FIS transfers. Counters related to events that occur during FIS transfers may count events related to host-to-device FIS transfers, device-to-host FIS transfers, or bi-directional FIS transfers. A counter that records bi-directional events is not required to be the sum of the counters that record the same events that occur on device-to-host FIS transfers and host-to-device FIS transfers.

Implementations that support Phy event counters shall implement all mandatory counters, and may support any of the optional counters as shown in 0. Note that some counters may increment differently based on the speed at which non-Data FIS retries are performed by the host and device. Implementations may record CRC and non-CRC error events differently. For example, there is a strong likelihood that a disparity error may cause a CRC error. Thus, the disparity error may cause both the event counter that records non-CRC events and the event counter that records CRC events to be incremented for the same event. Another example implementation difference is how a missing EOF event is recorded; a missing EOF primitive may imply a bad CRC even though the CRC on the FIS may be correct. These examples illustrate that some Phy event counters are sensitive to the implementation of the counters themselves, and thus these implementation sensitive counters cannot be used as an absolute measure of interface quality between different implementations.

8.20.3.1 Counter Reset Mechanisms

There are two mechanisms by which the host can explicitly cause the Phy counters to be reset.
The first mechanism is to issue a BIST Activate FIS to the device. Upon reception of a BIST Activate FIS the device shall reset all Phy event counters to their reset value. The second mechanism uses the READ LOG EXT command. When the device receives a READ LOG EXT command for log page 11h and bit 0 in the Features register is set to one, the device shall return the current counter values for the command and then reset all Phy event counter values.

8.20.3.2 Counter Identifiers

Each counter begins with a 16-bit identifier. 0 defines the counter value for each identifier. Any unused counter slots in the log page should have a counter identifier value of 0h.
Optional counters that are not implemented shall not be returned in log page 11h. A value of '0' returned for a counter means that there have been no instances of that particular event. There is no required ordering for event counters within the log page; the order is arbitrary and selected by the device vendor.

For all counter descriptions, ‘transmitted’ refers to items sent by the device to the host and ‘received’ refers to items received by the device from the host.

Bits 14:12 of the counter identifier convey the number of significant bits that counter uses. All counter values consume a multiple of 16-bits. The valid values for bits 14:12 and the corresponding counter sizes are:

1h 16-bit counter
2h 32-bit counter
3h 48-bit counter
4h 64-bit counter

Any counter that has an identifier with bit 15 set to one is vendor specific. This creates a vendor specific range of counter identifiers from 8000h to FFFFh. Vendor specific counters shall observe the number of significant bits 14:12 as defined above.

Identifier (Bits 11:0)	Mandatory / Optional	Description
000h	Mandatory	No counter value; marks end of counters in the page
001h	Mandatory	Command failed and ICRC bit set to one in Error register
002h	Optional	Not supported (R_ERR response for Data FIS)
003h	Optional	Not supported (R_ERR response for Device-to-Host Data FIS)
004h	Optional	Not supported (R_ERR response for Host-to-Device Data FIS)
005h	Optional	Not supported (R_ERR response for Non-data FIS)
006h	Optional	Not supported (R_ERR response for Device-to-Host Non-data FIS)
007h	Optional	Not supported (R_ERR response for Host-to-Device Non-data FIS)
008h	Optional	Not supported (Device-to-Host non-Data FIS retries)
009h	Optional	Transitions from drive PhyRdy to drive PhyNRdy
00Ah	Mandatory	Signature Device-to-Host Register FISes sent due to a COMRESET
00Bh	Optional	CRC errors within a Host-to-Device FIS
00Dh	Optional	Non-CRC errors within a Host-to-Device FIS
00Fh	Optional	Not supported (R_ERR response for Host-to-Device Data FIS due to CRC errors)
010h	Optional	Not supported (R_ERR response for Host-to-Device Data FIS due to non-CRC errors)
012h	Optional	Not supported (R_ERR response for Host-to-Device Non-data FIS due to CRC errors)
013h	Optional	Not supported (R_ERR response for Host-to-Device Non-data FIS due to non-CRC errors)

Table 52 Phy Event Counter Identifiers

8.20.3.2.1 Counter Definitions

The counter definitions in this section specify the events that a particular counter identifier represents.

8.20.3.2.1.1 Identifier 000h

There is no counter associated with identifier 000h. A counter identifier of 000h indicates that there are no additional counters in the log page.

8.20.3.2.1.2 Identifier 001h

The counter with identifier 001h returns the number of commands that returned an ending status with the ERR bit set to one in the Status register and the ICRC bit set to one in the Error register.

8.20.3.2.1.3 Identifier 009h

The counter with identifier 009h returns the number of times the device transitioned into the PHYRDY state from the PHYNRDY state, including but not limited to asynchronous signal events, power management events, and COMRESET events. If interface power management is enabled,

then this counter may be incremented due to interface power management transitions.

8.20.3.2.1.4 Identifier 00Ah

The counter with identifier 00Ah returns the number of transmitted Device-to-Host Register FISes with the device reset signature in response to a COMRESET, which were successfully followed by an R_OK from the host.

8.20.3.2.1.5 Identifier 00Bh

The counter with identifier 00Bh returns the number of received Host-to-Device FISes of all types (Data and non-Data) to which the device responded with R_ERRP due to CRC error.

8.20.3.2.1.6 Identifier 00Dh

The counter with identifier 00Dh returns the number of received Host-to-Device FISes of all types (Data and non-Data) to which the devices responded with R_ERRP for reasons other than CRC error.

8.20.3.3 READ LOG EXT Log Page 11h

READ LOG EXT log page 11h is one page (512 bytes) in length. The first Dword of the log page contains information that applies to the rest of the log page. Software should continue to process counters until a counter identifier with value 0h is found or the entire page has been read. A counter identifier with value 0h indicates that the log page contains no more counter values past that point. Log page 11h is defined in 0.

Byte	7	6	5	4	3	2	1	0
0	Reserved							
1	Reserved							
2	Reserved							
3	Reserved							
…	…							
n	Counter n Identifier							
n+1								
n+2	Counter n Value							
n + Counter n Length								
…	…							
508	Reserved							
509								
510								
511	Data Structure Checksum							

Table 53 READ LOG EXT Log Page 11h data structure definition

Counter n Identifier

Phy event counter identifier that corresponds to Counter n Value. Specifies the particular event counter that is being reported. The Identifier is 16 bits in length.
Valid identifiers are listed in 0.

Counter n Value

Value of the Phy event counter that corresponds to Counter n Identifier. The number of significant bits is determined by Counter n Identifier bits 14:12 (as defined in section 4.3.2). The length of Counter n Value shall always be a multiple of 16-bits. All counters are one-extended. For example, if a counter is only physically implemented as 8-bits when it reaches the maximum value of 0xFF, it shall be one-extended to 0xFFFF. The counter shall stop (and not wrap to zero) after reaching its maximum value.

Counter n Length

Size of the Phy event counter as defined by bits 14:12 of Counter n Identifier.
The size of the Phy event counter shall be a multiple of 16-bits.

Data Structure Checksum

The data structure checksum is the 2's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic and overflow shall be ignored. The sum of all 512 bytes of the data structure will be zero when the checksum is correct.

Reserved All reserved fields shall be cleared to zero

8.21 SCT Command Transport feature Set

8.21.1 Overview

8.21.1.1 Introduction

SMART Command Transport (SCT) is the method for the drive to receive commands using log page E0h and transporting data using log page E1h. These log pages are used as follows:

	Log page E0h	Log Page E1h
Write log page	Issue Command	Send Data to the drive
Read log page	Return Status	Received Data from the drive

Table 54 SCT Log Page and direction

There are two ways to access the log pages: using SMART READ/WRITE LOG and READ/WRITE LOG EXT. Both sets of commands access the same log pages and provide the same capabilities.

The log directory for log pages E0h and E1h should report a length of one. The length of log page E1h does not indicate the length of an SCT data transfer.

If SMART is supported, but not enabled, the drive supports SMART READ/WRITE LOG for Log page E0h and E1h.

If security is enabled and password has not been issued to unlock the device, all SCT commands will fail.

8.21.1.2 Capability definition

Capability Identification is performed by issuing Identify Device command. Word 206 of Identify Data is used to determine if SCT is enabled and which SCT Action Codes are supported.

Word	Description	
206	SCT Command set support	
	15-12	Vendor Specific
	11-6	Reserved
	5	Action Code 5 (SCT Data Table) supported
	4	Action Code 4 (Features Control) supported
	3	Action Code 3 (Error Recovery Control) supported
	2	Action Code 2 (LBA Segment Access) supported
	1	Action Code 1 (Long Sector Access) supported
	0	SCT Feature Set supported (includes SCT status)

Table 55 Identify Device Information Word 206

8.21.1.3 SCT Command Nesting and intermingling with Standard commands

In general, standard ATA commands can be intermingled with SCT Commands but SCT commands cannot be nested. SCT commands that do not require a follow-on data transfer operation never have an issue with being intermixed with any ATA commands or each other. SCT commands that do require data transfer, on the other hand, may not be nested; that is, if a key command that requires a data transfer is issued, all data transfer - to or from the host - must complete before another SCT command is issued. In most cases, however, ATA read/write commands may be inserted in between SCT data transfers, that is, between

complete SMART Read Log/Write Log commands. Furthermore, any reset (power-on, software or hardware) will cause the SCT command to be aborted.

8.21.1.4 Resets

If an SCT command is executing, any reset including Soft Reset, Hard Reset, COMRESET, and Power-On Reset all cause the command to be terminated. This could result in partial command execution or data loss. There is no indication once the drive becomes ready that the previous command was terminated.

8.21.2 SCT Command Protocol

8.21.2.1 Command Transport

SCT Command Transport occurs when a 512-byte data packet (called “Key Sector”) is created and the written to SMART or extended log page E0h. The key sector specifies Action and Function Codes along with the parameters that are required to perform the action.

8.21.2.1.1 Issue SCT Command Using SMART

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Feature	D6h							
Sector Count	01h							
Sector Number	E0h							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	-	-	-	D	-	-	-	-
Command	B0h							

Table 56 Output Registers of SCT Command Using SMART

Command Block Input Registers (Success)								
Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Depends on command (LSB)							
Sector Number	Depends on command (MSB)							
Cylinder Low	Number of sectors to transfer (LSB)							
Cylinder High	Number of sectors to transfer (MSB)							
Device/Head	-	-	-	-	-	-	-	-
Status	50h							

Command Block Input Registers (Error)								
Register	7	6	5	4	3	2	1	0
Error	04h							
Sector Count	Extended Status code (LSB)							
Sector Number	Extended Status code (MSB)							
Cylinder Low	Number of sectors to transfer (LSB)							
Cylinder High	Number of sectors to transfer (MSB)							
Device/Head	-	-	-	-	-	-	-	-
Status	51h							

Table 57 Input Registers of SCT Command Using SMART

8.21.2.1.2 Issue SCT Command Using Write Log Ext

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Feature	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	01h							
	Previous	00h							
LBA Low	Current	E0h							
	Previous	Reserved							
LBA Mid	Current	00h							
	Previous	00h							
LBA High	Current	Reserved							
	Previous	Reserved							
Device/Head		-	-	-	D	-	-	-	-
Command		3Fh							

Table 58 Input Registers of SCT Command Using Write Log Ext

Command Block Input Registers (Success)									
Register		7	6	5	4	3	2	1	0
Error		00h							
Sector Count	HOB=0	Depends on command (LSB)							
	HOB=1	Reserved							
LBA Low	HOB=0	Depends on command (MSB)							
	HOB=1	Reserved							
LBA Mid	HOB=0	Number of sectors (LSB)							
	HOB=1	Reserved							
LBA High	HOB=0	Number of sectors (MSB)							
	HOB=1	Reserved							
Device/Head		-	-	-	-	-	-	-	-
Status		50h							

Command Block Input Registers (Error)									
Register		7	6	5	4	3	2	1	0
Error		04h							
Sector Count	HOB=0	Extended Status Code (LSB)							
	HOB=1	Reserved							
LBA Low	HOB=0	Extended Status Code (MSB)							
	HOB=1	Reserved							
LBA Mid	HOB=0	Number of sectors (LSB)							
	HOB=1	Reserved							
LBA High	HOB=0	Number of sectors (MSB)							
	HOB=1	Reserved							
Device/Head		-	-	-	-	-	-	-	-
Status		51h							

All ATA “previous” registers are reserved in Write Log Ext responses.

Table 59 Output Registers of SCT Command Using Write Log Ext

8.21.2.1.3 Key Sector Format

An SCT command (Key Sector) is always 512 bytes long. Table below shows the generic format of an SCT command.

Byte	Field	Words	Description
1:0	Action Code	1	This field defines the command type and generally specifies the type of data being accessed, such as sector or physical action being performed, such as seek.
3:2	Function Code	1	This field specifies the type of access, and varies by command. For example, this can specify read, write, verify, etc.
X:4	Parameter1	Depends on command	Depends on command
Y:x+1	Parameter2	Depends on command	Depends on command
…	…	…	…
	Total Words	256	

Table 60 Key Sector Format

The action codes are defined in Table below.

Action Code	Block Data	TF Data	Description
0000h	-	-	Reserved
0001h	Read/Write	Y	Long Sector Access (Not Supported)
0002h	Write	N	LBA Segment Access
0003h	-	Y	Error Recovery Control
0004h	-	Y	Features Control
0005h	Read	N	SCT Data Table
0006h-BFFFh	-	-	Reserved
C000h-FFFFh	-	-	Vendor Specific

Table 61 SCT Action Code List

8.21.2.1.4 Extended Status Code

Status Code	Definition
0000h	Command complete without error
0001h	Invalid Function Code
0002h	Input LBA out of range
0003h	Request sector count overflow. The number of sectors requested to transfer (Sector Count register) in the read or write log command is larger than required by SCT command.
0004h	Invalid Function code in Error Recovery command
0005h	Invalid Selection code in Error Recovery command
0006h	Host read command timer is less than minimum value
0007h	Host write command timer is less than minimum value
0008h	Background SCT command was aborted because of an interrupting host command
0009h	Background SCT command was terminated because of unrecoverable error
000Ah	Invalid Function code in Long Sector Access command
000Bh	SCT data transfer command was issued without first issuing an SCT command
000Ch	Invalid Function code in Feature Control command
000Dh	Invalid Feature code in Feature Control command
000Eh	Invalid New State value in Feature Control command
000Fh	Invalid Option Flags in Feature Control command
0010h	Invalid SCT Action code
0011h	Invalid Table ID (table not supported)
0012h	Command was aborted due to drive security being locked
0013h	Invalid revision code
0017h	Blocking SCT Segment Access command was terminated because of unrecoverable error
0018h-BFFFh	Reserved
C000h-C002h	Vendor Specific
C003h	Overlay switch failure in Long Sector Access command
C004h	Read Long failure
C005h	Write Long failure
C006h	Write Cache enable failure
C007h-FFEFh	Vendor Specific
FFF0h-FFFEh	Reserved
FFFFh	SCT command executing in background

Table 62 Extended Status Code

8.21.2.2 Data transfer

Once an SCT command has been issued, status can be checked and data can be transferred. Data transfer uses log page E1h.

8.21.2.2.1 Read/Write SCT Data Using SMART

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Feature		D5h(Read)/D6h(Write)							
Sector Count		Number of sectors to be transferred							
Sector Number		E1h							
Cylinder Low		4Fh							
Cylinder High		C2h							
Device/Head		-	-	-	D	-	-	-	-
Command		B0h							

Table 63 Input Registers of SCT Data Transfer Using SMART

8.21.2.2.2 Read/Write SCT Data Using Read/Write Log Ext

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Feature	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	01h							
	Previous	00h							
LBA Low	Current	E1h							
	Previous	Reserved							
LBA Mid	Current	00h							
	Previous	00h							
LBA High	Current	Reserved							
	Previous	Reserved							
Device/Head		-	-	-	D	-	-	-	-
Command		2Fh(Read)/3Fh(Write)							

Table 64 Input Registers of SCT Data Transfer using Read/Write Log Ext

8.21.2.3 SCT Status Request

Once an SCT command has been issued, a status is reported in the ATA registers. This status indicates that the command was accepted or that an error occurred. This ATA status return does not indicate successful completion of the SCT actions. Some commands can take several minutes or even hours to execute. In this case, the host can determine execution progress by requesting SCT status.

Log page E0h contains the status information. Reading log page E0h retrieves the status information. The SCT status may be acquired any time that the host is allowing to send a command to the device. This command will not change the power state of the drive, nor terminate any background activity, including any SCT command in progress.

8.21.2.3.1 SCT Status Request Using SMART

Command Block Output Registers									
Register	7	6	5	4	3	2	1	0
Feature	D5h							
Sector Count	01h							
Sector Number	E0h							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	-	-	-	D	-	-	-	-
Command	B0h							

Table 65 Intput Registers of SCT Status Request Using SMART

8.21.2.3.2 SCT Status Request Using Read Log Ext

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Feature	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	01h							
	Previous	00h							
LBA Low	Current	E0h							
	Previous	Reserved							
LBA Mid	Current	00h							
	Previous	00h							
LBA High	Current	Reserved							
	Previous	Reserved							
Device/Head		-	-	-	D	-	-	-	-
Command		2Fh							

Table 66 Input Registers of SCT Status Request Using Read Log Ext

8.21.2.3.3 Format of SCT Status Response

Byte	Type	Field Name	Value	Description
1:0	Word	Format Version	0003h	Status Response format version number
3:2	Word	SCT Version		Manufacturer's vendor specific implementation version number
5:4	Word	SCT Spec.	0001h	Highest level of SCT Technical Report supported
9:6	DWord	Status Flags		Bit 0 : Segment Initialized Flag If this bit is set to 1, an LBA Segment Access command write to all LBAs of the drive has completed without error. This bit shall be cleared to 0 when any user LBA is written, even if write cache is enabled. This bit is alse cleared if the capacity of the drive is changed via SETMAX, SETMAX EXT or DCO. This bit is preserved through a power cycle. Bit 1-31 : Reserved
10	Byte	Drive Status		0 = Active waiting for a command 1 = Stand-by 2 = Sleep 3 = DST executing in background 4 = SMART ODC executing in background 5 = SCT executing in background
13:11	Byte[3]	reserved	00h	
15:14	Word	Extended Status Code		Status Of last SCT command issued. FFFFh if SCT command executing in background.
17:16	Word	Action Code		Action code of last SCT command issued. If the Extended Status Code is FFFFh, this is the Action Code of the command that is current executing.
19:18	Word	Function Code		Function code of last SCT command issued. If the Extended Status Code is FFFFh, this is the Function Code of the command that is current executing.
39:20	Byte[20]	reserved	00h	
47:40	QWord	LBA		Current LBA of SCT command executin in background. If there is no command currently executing in the background, this field is undefined.
199:48	Byte[152]		00h	
200	Byte	HDA Temp		Current HDA temperature in degrees Celsius. This is a 2's complement number. 80h indicates that this value is invalid.
201	Byte	Min Temp		Minimum HDA temperature in degrees Celsius. This is a 2's complement integer. 80h indicates that this value is invalid.
202	Byte	Max Temp		Maximum HDA temperature in degrees Celsius. This is a 2's complement number. 80h indicates that this value is invalid.
203	Byte	Life Min Temp		Minimum HDA temperature in degrees Celsius seen for the life of the device. This is a 2's complement integer. 80h indicates that this value is invalid.
204	Byte	Life Max Temp		Maximum HDA temperature in degrees Celsius seen for the life of the drive. This is a 2's complement number. 80h indicates that this value is invalid.

205	Byte	Reserved	00h	
209:206	Dword	Over Limit Count		Number of temperature recording Intervals since the last power-on reset where the recorded temperature was greater than Max Op Limit. See table 93 for information about this Interval.
213:210	Dword	Under Limit Count		Number of temperature recording Intervals since the last power-on reset where the recorded temperature was less than Min Op Limit. See table 93 for information about this Interval.
479:214	Byte[275]	Reserved	00h	
511:480	Byte[32]	Vendor Specific	00h	

Table 67 Data Format of SCT Status Response

8.21.3 SCT Command Set

8.21.3.1 LBA Segment Access (action code : 0002h)

Inputs: (Key Sector)

Word	Name	Value	Description
0	Action Code	0002h	This action writes a pattern or sector of data repeatedly to the media. This capability could also be referred to as “Write All” or “Write Same”.
1	Function Code	0001h	Repeat Write Pattern (Background Operation)
		0002h	Repeat Write Sector (Background Operation)
		0101h	Repeat Write Pattern (Blocking Operation)
		0102h	Repeat Write Sector (Blocking Operation)
5:2	Start LBA	QWord	First LBA
9:6	Count	QWord	Number of sectors to fill
11:10	Pattern	DWord	If the Function Code is 0001h, this field contains a 32-bit pattern that is written on the media starting at the location specified in words two through five
255:12	reserved	0000h	

Table 68 LBA Segment Access (Inputs)

Outputs: (TF Data)

Command Block Input Registers (Success)	
Error	00h
Sector Count	Reserved
Sector Number	Reserved
Cylinder Low	Number of sectors to transfer (LSB) = 01h
Cylinder High	Number of sectors to transfer (MSB) = 00h
Device/Head	reserved
Status	50h

Table 69 LBA Segment Access (Outputs)

The LBA Segment Access command will begin writing sectors from Start LBA in incrementing order until Count sectors have been written. A Count of zero means apply operation from Start LBA until the last user LBA on the drive is reached. The HPA feature determines the last user LBA. This command will not write over a hidden partition when hidden partitions are enabled using the Host Protected Area drive capabilities. Automatic sector reassignment is permitted during the operation of this function.

If Start LBA or Start LBA + Count go beyond the last user LBA then an error is reported and the SCT command is not executed. Issuing this command with a value of zero for Start LBA and Count will cause all LBAs of the drive to be written the specified pattern.

Once the key sector has been issued, if the Function Code was 0002h or 0102h and the TF Data indicates that the drive is ready to receive data, log page E1h should be written to transfer the data.

This command can change the Segment Initialized Flag. If the command writes all the user addressable sectors and completes without encountering an error or being aborted, then the “Segment Initialized Flag” (bit 0 of the Status Flags in the SCT Status. See0) shall be set to 1. A write to any user addressable sector on the drive (except another complete write all), shall cause the Segment Initialized Flag to be cleared. Reallocations as a result of reading data (foreground or background) do not clear the Segment Initialized Flag.

Implementation note for Background Operation (Function code = 0001h, 0002h)

In this mode, the drive will return command completion status when the drive finished receiving data.

Any command, including IDENTIFY DEVICE, other than SCT Status, issued to the drive while this command is in progress will terminate the LBA Segment Access command. The incoming command is executed.

Use the SCT Status command to retrieve status information about the current SCT command. Example status information includes: command active or complete, current LBA, and errors. When this command is in progress, the SCT status error code will be FFFFh, and set to 0000h if the command completes without error. It will be less than FFFFh and grater the 0000h if the command terminated prematurely for any reason.

Possible Extended Status Code for Background Operation (Function code = 0001h, 0002h)	
0008h	Background SCT command was aborted because of an interrupting host command
0009h	Background SCT command was terminated because of unrecoverable error
FFFFh	SCT command executing in background

Implementation note for Blocking Operation (Function code = 0101h, 0102h)

In this mode, the drive will return command completion status when the drive finished the LBA Segment Access operation.

Outputs for Error

Command Block Input Registers (Error)								
Register	7	6	5	4	3	2	1	0
Error	04h							
Sector Count	Extended Status code (LSB)							
Sector Number	Extended Status code (MSB)							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	-	-	-	-	-	-	-	-
Status	51h							

Possible Extended Status Code for Blocking Operation (Function code = 0101h, 0102h)	
0017h	Blocking SCT Segment Access command was terminated because of unrecoverable error

8.21.3.2 Error Recovery Control command (action code : 0003h)

Inputs: (Key Sector)

Word	Name	Value	Description
0	Action Code	0003h	Set the read and write error recovery time
1	Function Code	0001h	Set New Value
		0002h	Return Current Value
2	Selection Code	0001h	Read Timer
		0002h	Write Timer
3	Value	Word	If the function code is 0001h, then this field contains the recovery time limit in 100ms units. The minimum SCT timeout value is 65 (=6.5 second). When the specified time limit is shorter than 6.5 second,the issued command is aborted.
255:4	reserved	0000h	

Table 70 Error Recovery Control command (Inputs)

Outputs: (TF Data)

Command Block Input Registers (Success)	
Error	00h
Sector Count	If Function Code was 0002h, then this is the LSB of the requested recovery limit. Otherwise, this field is reserved.
Sector Number	If Function Code was 0002h, then this is the MSB of the requested recovery limit. Otherwise, this field is reserved.
Cylinder Low	reserved
Cylinder High	reserved
Device/Head	reserved
Status	50h

Table 71 Error Recovery Control command (Onputs)

The Error Recovery Control command can be used to set time limits for read and write error recovery. For non-queued commands, these timers apply to command completion at the host interface. For queued commands where in order data delivery is enabled, these timers begin counting when the device begins to execute the command, not when the command is sent to the device. These timers do not apply to streaming commands, or to queued commands when out-of-order data delivery is enabled.

These command timers are volatile. The default value is 0 (i.e. disable command time-out).

8.21.3.3 Feature Control Command (action code : 0004h)

Inputs: (Key Sector)

Word	Name	Value	Description
0	Action Code	0004h	Set or return the state of drive features described in 0
1	Function Code	0001h	Set state for a feature
		0002h	Return the current state of a feature
		0003h	Return feature option flags
2	Feature Code	Word	See 0 for a list of the feature codes
3	State	Word	Feature code dependent value
4	Option Flags	Word	Bit15:1 = Reserved If the function code is 0001h, setting bit 0 to one causes the requested feature state change to be preserved across power cycles. If the function code is 0001h, setting bit 0 to zero causes the requested feature state change to be volatile. A hard reset causes the drive to revert to default, or last non-volatile setting.
255:5	reserved	0000h	

Table 72 Feature Control command (Inputs)

Outputs: (TF Data)

Command Block Input Registers (Success)	
Error	00h
Sector Count	If Function Code was 0002h, then this is the LSB of Feature State. If Function Code was 0003h, then this is the LSB of Option Flags. Otherwise, this field is reserved.
Sector Number	If Function Code was 0002h, then this is the MSB of Feature State. If Function Code was 0003h, then this is the MSB of Option Flags. Otherwise, this field is reserved.
Cylinder Low	reserved
Cylinder High	reserved
Device/Head	reserved
Status	50h

Table 73 Feature Control command (Outputs)

Feature Code	State Definition
0001h	0001h : Allow write cache operation to be determined by Set Feature command 0002h : Force write cache enabled 0003h : Force write cache disabled If State 0001h is selected, the ATA Set Feature command will determine the operation state of write cache. If State 0002h or 0003h is selected, write cache will be forced into the corresponding operation state, regardless of the current ATA Set Feature state. Any attempt to change the write cache setting through Set Feature shall be accepted, but otherwise ignored, and not affect the operation state of write cache and complete normally without reporting an error. In all cases, bit 5 of word 85 in the Identify Device information will reflect the true operation state of write cache, one indicating enabled and zero indicating disabled. The default state is 0001h.
0002h	0001h : Enable Write Cache Reordering 0002h : Disable Write Cache Reordering The default state is 0001h. The drive does not return error for setting state 0002h, but the state is ignored.
0003h	Set time interval for temperature logging. 0000h is invalid. 0001h to FFFFh logging interval in minutes. This value applies to the Absolute HDA Temperature History queue. Issuing this command will cause the queue to be reset and any prior values in the queue will be lost. Queue Index shall be set to zero and the first queue location will be set to the current value. All remaining queue locations are set to 80h. The Sample Period, Max Op Limit, Over Limit, Min Op Limit and Under Limit values are preserved. Default value is 0001h.
0004h-CFFFh	Reserved
D000h-FFFFh	Vendor Specific

Table 74 Feature Code List

8.21.3.4 SCT Data Table Command (action code : 0005h)

Inputs: (Key Sector)

Word	Name	Value	Description
0	Action Code	0005h	Read a data table
1	Function Code	0001h	Read Table
2	Table ID	Word	See 0 for a list of data tables
255:2	reserved	0000h	

Table 75 SCT Data Table command (Inputs)

Outputs: (TF Data)

Command Block Input Registers (Success)	
Error	00h
Sector Count	reserved
Sector Number	reserved
Cylinder Low	Number of sectors to transfer (LSB) = 01h
Cylinder High	Number of sectors to transfer (MSB) = 00h
Device/Head	reserved
Status	50h

Table 76 SCT Data Table command (Outputs)

Table ID	Description
0000h	Invalid
0001h	Reserved
0002h	HDA Temperature History Table (in absolute degree C). See 0
0003h-CFFFh	Reserved
D000h-FFFFh	Vendor Specific

Table 77 Table ID

Byte	Size	Field Name	Description
1:0	Word	Format Version	Data table format version (=0002h)
3:2	Word	Sampling Period	Absolute HDA Temperature sampling period in minutes. 0000h indicates sampling is disabled.
5:4	Word	Interval	Timer interval between entries in the history queue.
6	Byte	Max Op Limit	Maximum recommended continuous operating temperature. This is a one byte 2's complement number that allows a range from -127°C to +127°C to be specified. 80h is an invalid value. This is a fixed value.
7	Byte	Over Limit	Maximum temperature limit. This is a one byte 2's complement number that allows a range from -127°C to +127°C to be specified. 80h is an invalid value. This is a fixed value.
8	Byte	Min Op Limit	Minimum recommended continuous operating limit. This is a one byte 2's complement number that allows a range from -127°C to +127°C to be specified. 80h is an invalid value. This is a fixed value.
9	Byte	Under Limit	Minimum temperature limit. This is a one byte 2's complement number that allows a range from -127°C to +127°C to be specified. 80h is an invalid value. This is a fixed value.
29:10	Byte[20]	Reserved	
31:30	Word	Queue Size	Number of entry locations in history queue. This value is 128.
33:32	Word	Queue Index	Last updated entry in queue. Queue Index is zero-based, so Queue Index 0000h is the first location in the buffer (at offset 34). The most recent temperature entered in the buffer is at Queue Index + 34. See Note 1 and Note 2.

(Queue Size+33):34	Byte[Queue Size]	Queue Buffer	This is a circular buffer of absolute HDA Temperature values. These are one byte 2's complement numbers, which allow a range from -127°C to +127°C to be specified. A value of 80h indicates an initial value or a discontinuity in temperature recording. The Actual time between samples may vary because commands may not be interrupted. The sampling period is the minimum time between samples. See Not 1. If the host changes the logging interval using the volatile option, the interval between entries in the queue may change between power cycles with no indication to the host.
511:(Queue Size +34)	Byte[512-Queue Size-34]	Reserved	
Note 1 – The Absolute HDA Temperature History is preserved across power cycles with the requirement that when the drive powers up, a new entry is made in the history queue of 80h, an invalid absolute temperature value. This way an application viewing the history can see the discontinuity in temperature result from the drive being turned off. Note 2 – When the Absolute HDA Temperature history is cleared, for new drives or after changing the Logging Interval, the Queue Index shall be set to zero and the first queue location shall be set to the current Absolute HDA Temperature value. All remaining queue locations are set to 80h.			

Table 78 Data Format of HDA Absolute Temperature History Table

9.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

Please refer to Serial ATA Revision 1.0a (Section 9. device command layer protocol) and Serial ATA II: Extensions to Serial ATA 1.0a (Section 4. Command layer) about each protocol.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a COMRESET or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

The device timeout values are described in the Section 11.0 on the page 266.

9.1 PIO Data In commands

These commands are:

- Device Configuration Identify
- Identify Device
- Read Buffer
- Read Log Ext
- Read Multiple
- Read Multiple Ext
- Read Sector(s)
- Read Sector(s) Ext
- Read Stream PIO
- SMART Read Attribute Values
- SMART Read Attribute Thresholds
- SMART Read Log Sector

Execution includes the transfer of one or more 512 byte sectors of data from the device to the host.

9.2 PIO Data Out commands

These commands are:

- Device Configuration Set
- Download Microcode
- Format Track
- Security Disable Password
- Security Erase Unit
- Security Set Password
- Security Unlock
- Set Max Set Password command
- Set Max Unlock command
- SMART Write Log Sector
- Write Buffer
- Write Log Ext
- Write Multiple
- Write Multiple Ext

- Write Multiple FUA Ext
- Write Sector(s)
- Write Sector(s) Ext
- Write Stream PIO

Execution includes the transfer of one or more 512 byte sectors of data from the host to the device.

9.3 Non-Data commands

These commands are:

- Check Power Mode
- Configure Stream
- Device Configuration Freeze Lock
- Device Configuration Restore
- Execute Device Diagnostic
- Flush Cache
- Flush Cache Ext
- Idle
- Idle Immediate
- Initialize Device Parameters
- NOP
- Read Native Max Address
- Read Native Max Address Ext
- Read Verify Sector(s)
- Read Verify Sector(s) Ext
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Set Features
- Set Max Address
- Set Max Address Ext
- Set Max Lock command
- Set Max Freeze Lock command
- Set Multiple Mode
- Sleep
- SMART Disable Operations
- SMART Enable/Disable Attribute Autosave
- SMART Enable Operations
- SMART Execute Off-line Data Collection
- SMART Return Status
- SMART Save Attribute Values
- SMART Enable/Disable Automatic Off-Line
- Standby
- Standby Immediate
- Write Uncorrectable Ext

Execution of these commands involves no data transfer.

9.4 DMA Data In commands and DMA Data Out commands

These commands are:

- Read DMA
- Read DMA Ext
- Read Stream DMA
- Write DMA
- Write DMA Ext
- Write DMA FUA Ext
- Write Stream DMA

Execution of this class of command includes the transfer of one or more blocks of data between the device and

the host using DMA transfer.

9.5 First-party DMA commands

These commands are:

- Read FPDMA Queued
- Write FPDMA Queued

Execution of this class of commands includes command queuing and the transfer of one or more blocks of data between the device and the host. The protocol is described in the section 4.2 “Native Command Queuing” of “Serial ATA II: Extensions to Serial ATA 1.0a”.

Host knowledge of I/O priority may be transmitted to the device as part of the command. There are two priority classes for NCQ command as high priority, the host is requesting a better quality of service for that command than the commands issued with normal priority.

The classes are forms of soft priority. The device may choose to complete a normal priority command before an outstanding high priority command, although preference shallbe given to the high priority commands. The priority class is indicated in bit 7 (Priority Information) in the Sector Count register for NCQ commands (READ FPDMA QUEUED and WRITE FPDMA QUEUED). This bit can indicate either the normal priority or high priority class. If a command is marked by the host as high priority, the device shall attempt to provide better quality of service for the command. It is not required that devices process all high priority requests before satisfying normal priority requests.

10.0 Command Descriptions

Protocol	Command	Code (Hex)	Binary Code Bit							
			7	6	5	4	3	2	1	0
3	Check Power Mode	E5	1	1	1	0	0	1	0	1
3	Check Power Mode*	98	1	0	0	1	1	0	0	0
3	Configure Stream	51	0	1	0	1	0	0	0	1
3	Device Configuration Restore	B1	1	0	1	1	0	0	0	1
3	Device Configuration Freeze Lock	B1	1	0	1	1	0	0	0	1
1	Device Configuration Identify	B1	1	0	1	1	0	0	0	1
2	Device Configuration Set	B1	1	0	1	1	0	0	0	1
2	Download Microcode	92	1	0	0	1	0	0	1	0
3	Execute Device Diagnostic	90	1	0	0	1	0	0	0	0
3	Flush Cache	E7	1	1	1	0	0	1	1	1
3	Flush Cache Ext	EA	1	1	1	0	1	0	1	0
2	Format Track	50	0	1	0	1	0	0	0	0
1	Identify Device	EC	1	1	1	0	1	1	0	0
3	Idle	E3	1	1	1	0	0	0	1	1
3	Idle*	97	1	0	0	1	0	1	1	1
3	Idle Immediate	E1	1	1	1	0	0	0	0	1
3	Idle Immediate*	95	1	0	0	1	0	1	0	1
3	Initialize Device Parameters	91	1	0	0	1	0	0	0	1
1	Read Buffer	E4	1	1	1	0	0	1	0	0
4	Read DMA	C8	1	1	0	0	1	0	0	0
4	Read DMA	C9	1	1	0	0	1	0	0	1
4	Read DMA Ext	25	0	0	1	0	0	1	0	1
5	Read FPDMA Queued	60	0	1	1	0	0	0	0	0
1	Read Log Ext	2F	0	0	1	0	1	1	1	1
1	Read Multiple	C4	1	1	0	0	0	1	0	0
1	Read Multiple Ext	29	0	0	1	0	1	0	0	1
3	Read Native Max Address	F8	1	1	1	1	1	0	0	0
3	Read Native Max Address Ext	27	0	0	1	0	0	1	1	1
1	Read Sector(s)	20	0	0	1	0	0	0	0	0
1	Read Sector(s)	21	0	0	1	0	0	0	0	1
1	Read Sector(s) Ext	24	0	0	1	0	0	1	0	0
4	Read Stream DMA	2A	0	0	1	0	1	0	1	0
4	Read Stream PIO	2B	0	0	1	0	1	0	1	0
3	Read Verify Sector(s)	40	0	1	0	0	0	0	0	0
3	Read Verify Sector(s)	41	0	1	0	0	0	0	0	1
3	Read Verify Sector(s) Ext	42	0	1	0	0	0	0	1	0
3	Recalibrate	1x	0	0	0	1	-	-	-	-
2	Security Disable Password	F6	1	1	1	1	1	0	1	0
3	Security Erase Prepare	F3	1	1	1	1	0	0	1	1
2	Security Erase Unit	F4	1	1	1	1	0	1	0	0
3	Security Freeze Lock	F5	1	1	1	1	0	1	0	1
2	Security Set Password	F1	1	1	1	1	0	0	0	1
2	Security Unlock	F2	1	1	1	1	0	0	1	0

Table 79 Command Set

Protocol	Command	Code	Binary Code Bit							
		(Hex)	7	6	5	4	3	2	1	0
3	Seek	7x	0	1	1	1	-	-	-	-
3	Set Features	EF	1	1	1	0	1	1	1	1
3	Set Max Address	F9	1	1	1	1	1	0	0	1
3	Set Max Address Ext	37	0	0	1	1	0	1	1	1
3	Set Multiple Mode	C6	1	1	0	0	0	1	1	0
3	Sleep	E6	1	1	1	0	0	1	1	0
3	Sleep*	99	1	0	0	1	1	0	0	1
3	SMART Disable Operations	B0	1	0	1	1	0	0	0	0
3	SMART Enable/Disable Attribute Auto save	B0	1	0	1	1	0	0	0	0
3	SMART Enable Operations	B0	1	0	1	1	0	0	0	0
3	SMART Execute Off-line Data Collection	B0	1	0	1	1	0	0	0	0
1	SMART Read Attribute Values	B0	1	0	1	1	0	0	0	0
1	SMART Read Attribute Thresholds	B0	1	0	1	1	0	0	0	0
3	SMART Return Status	B0	1	0	1	1	0	0	0	0
3	SMART Save Attribute Values	B0	1	0	1	1	0	0	0	0
2	SMART Write Log Sector	B0	1	0	1	1	0	0	0	0
3	SMART Enable/Disable Automatic Off-line	B0	1	0	1	1	0	0	0	0
3	Standby	E2	1	1	1	0	0	0	1	0
3	Standby*	96	1	0	0	1	0	1	1	0
3	Standby Immediate	E0	1	1	1	0	0	0	0	0
3	Standby Immediate*	94	1	0	0	1	0	1	0	0
2	Write Buffer	E8	1	1	1	0	1	0	0	0
4	Write DMA	CA	1	1	0	0	1	0	1	0
4	Write DMA	CB	1	1	0	0	1	0	1	1
4	Write DMA Ext	35	0	0	1	1	0	1	0	1
4	Write DMA FUA Ext	3D	0	0	1	1	1	1	0	1
5	Write FPDMA Queued	61	0	1	1	0	0	0	0	1
2	Write Log Ext	3F	0	0	1	1	1	1	1	1
2	Write Multiple	C5	1	1	0	0	0	1	0	1
2	Write Multiple Ext	39	0	0	1	1	1	0	0	1
2	Write Multiple FUA Ext	CE	1	1	0	0	1	1	1	0
2	Write Sector(s)	30	0	0	1	1	0	0	0	0
2	Write Sector(s)	31	0	0	1	1	0	0	0	1
2	Write Sector(s) Ext	34	0	0	1	1	0	1	0	0
4	Write Stream DMA	3A	0	0	1	1	1	0	1	0
4	Write Stream PIO	3B	0	0	1	1	1	0	1	1
3	Write Uncorrectable Ext	45	0	1	0	0	0	1	0	1

Protocol :
1 : PIO data IN command
2 : PIO data OUT command
3 : Non data command
4 : DMA command
5 :
+ : Vendor specific command

Table 80 Command Set --Continued--

Commands marked * are alternate command codes for previous defined commands.

Command (Subcommand)	Command code (Hex)	Feature Register (Hex)
(SMART Function)		
SMART Read Attribute Values	B0	D0
SMART Read Attribute Thresholds	B0	D1
SMART Enable/Disable Attribute Autosave	B0	D2
SMART Save Attribute Values	B0	D3
SMART Execute Off-line Data Collection	B0	D4
SMART Read Log	B0	D5
SMART Write Log	B0	D6
SMART Enable Operations	B0	D8
SMART Disable Operations	B0	D9
SMART Return Status	B0	DA
SMART Enable/Disable Automatic Off-line	B0	DB
(Set Features)		
Enable Write Cache	EF	02
Set Transfer Mode	EF	03
Enable Advanced Power Management	EF	05
Enable Power-up in Standby Feature Set	EF	06
Power-up in Standby Feature Set Device Spin-up	EF	07
Enable Address Offset Mode	EF	09
Enable Automatic Acoustic Management	EF	42
Disable read look-ahead feature	EF	55
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Disable Advanced Power Management	EF	85
Disable Power-up in Standby Feature Set	EF	86
Disable Address Offset Mode	EF	89
Enable read look-ahead feature	EF	AA
Disable Automatic Acoustic Management	EF	C2
Enable reverting to power on defaults	EF	CC

Table 81 Command Set (Subcommand)

Table 78 Command Set on page 115 and **Table 79 Command Set --Continued--** on page 116 show the commands that are supported by the device. **Table 80** on page 117 shows the sub-commands those are supported by each command or feature.

The following symbols are used in the command descriptions:

Output Registers

0 Indicates that the bit must be set to 0.

1 Indicates that the bit must be set to 1.

D The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. This bit is reserved since all Serial ATA devices behave like Device 0.

H Head number. Indicates that the head number part of the Device/Head Register is an output parameter and should be specified.

L LBA mode. Indicates the addressing mode. Zero specifies CHS mode and one does LBA addressing mode.

R Retry. Original meaning is already obsoleted, there is no difference between 0 and 1. (Using 0 is recommended for future compatibility.)

B Option Bit. Indicates that the Option Bit of the Sector Count Register should be specified. (This bit is used by Set Max ADDRESS command)

V Valid. Indicates that the bit is part of an output parameter and should be specified.

x Indicates that the hex character is not used.

- Indicates that the bit is not used.

Input Registers

0 Indicates that the bit is always set to 0.

1 Indicates that the bit is always set to 1.

H Head number. Indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.

V Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.

- Indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

Please refer to ATA interface specifications about other commands' descriptions which are not described in this SATA interface specification. However, be careful that Serial ATA Device/Head register bit-4 (d) is different from that of Parallel ATA. In Serial ATA, Device/Head register bit-4 is reserved for all commands.

10.1 Check Power Mode (E5h/98h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-		-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 82 Check Power Mode Command (E5h/98h)

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input Parameters From The Device

Sector Count The power mode code. The command returns 0 in the Sector Count Register if the device is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0FFh.

10.2

10.3 Configure Stream (51h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	-	-	-	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	1	1	D	-	-	-	-
Command		0	1	0	1	0	0	0	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	SE	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 83 Configure Stream Command (51h)

The Configure Stream command specifies the operating parameters of an individual stream. A Configure Stream command may be issued for each stream that is to be added or removed from the current operating configuration. If A/R = 1 and the specified ID is already valid at the device, the new parameters shall replace the old parameters, unless Command Abort is returned (see abort conditions for Error Register). In this case the old parameters for the specified Stream ID shall remain in effect.

Output Parameters To The Device

Feature Current bit 7 (A/R)	If set to one, a request to add a new stream. If cleared to zero, a request to remove a previous configured stream is specified.
Feature Current bit 6 (R/W)	R/W specifies a read stream if cleared to zero and a write stream if set to one.
Feature Current bit 0..2 (Stream ID)	The Stream ID shall be a value between 0 and 7.
Feature Previous	The default Command Completion Time Limit (CCTL). The value is calculated as follows: (Default CCTL) = ((content of the Features register)* (Identify Device words (99:98))) micriseconds. This time shall be used by the device when a streaming command with the same stream ID and a CCTL of zero are issued. The time is measured from the write of the command register to the final INTRQ for command completion. The minimum CCTL is 50ms.CCTL is set to 50ms when the specified value is shorter than 50ms.
Sector Count Current	Allocation Unit Size In Sectors (7:0)
Sector Count Previous	Allocation Unit Size In Sectors (15:8)

10.4 Device Configuration Overlay (B1h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	1	0	1	0	V	V	V	V
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	D	-	-	-	-
Command	1	0	1	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	-	V	-	-	V

Table 84 Device Configuration Overlay Command (B1h)

Individual Device Configuration Overlay feature set commands are identified by the value placed in the Features register. The table below shows these Features register values.

Value	Command
C0h	DEVICE CONFIGURATION RESTORE
C1h	DEVICE CONFIGURATION FREEZE LOCK
C2h	DEVICE CONFIGURATION IDENTIFY
C3h	DEVICE CONFIGURATION SET
other	Reserved

Table 85 Device Configuration Overlay Features register values

10.4.1 Device Configuration Restore (Subcommand C0h)

The Device Configuration Restore command disables any setting previously made by a Device Configuration Set command and returns the content of the Identify Device or Identify Packet Device command response to the original settings as indicated by the data returned from the execution of a Device Configuration Identify command.

10.4.2 Device Configuration Freeze Lock (Subcommand C1h)

The Device Configuration Freeze Lock command prevents accidental modification of the Device Configuration Overlay settings. After successful execution of a Device Configuration Freeze Lock command, all Device Configuration Set, Device Configuration Freeze Lock, Device Configuration Identify, and Device Configuration Restore commands are aborted by the device. The Device Configuration Freeze Lock condition shall be cleared by a power-down. The Device Configuration Freeze Lock condition shall not be cleared by hardware or software reset.

10.4.3 Device Configuration Identify (Subcommand C2h)

The Device Configuration Identify command returns a 512 byte data structure via PIO data-in transfer. The content of this data structure indicates the selectable commands, modes, and feature sets that the device is capable of supporting. If a Device Configuration Set command has been issued reducing the capabilities, the response to an Identify Device or Identify Packet Device command will reflect the reduced set of capabilities, while the Device Configuration Identify command will reflect the entire set of selectable capabilities.

The format of the Device Configuration Overlay Data structure is shown on next page.

10.4.4 Device Configuration Set (Subcommand C3h)

The Device Configuration Set command allows a device manufacturer or a personal computer system manufacturer to reduce the set of optional commands, modes, or feature sets supported by a device as indicated by a Device Configuration Identify command. The Device Configuration Set command transfers an overlay that modifies some of the bits set in words 63, 82, 83, 84, and 88 of the Identify Device command response. When the bits in these words are cleared, the device no longer supports the indicated command, mode, or feature set. If a bit is set in the overlay transmitted by the device that is not set in the overlay received from a Device Configuration Identify command, no action is taken for that bit.

The format of the overlay transmitted by the device is described in the table on next page. The restrictions on changing these bits are described in the text following that table. If any of the bit modification restrictions described are violated or any setting is changed with Device Configuration Set command, the device shall return command aborted. At that case, error reason code is returned to sector count register, invalid word location is returned to cylinder high register, and invalid bit location is returned to cylinder low register. The Definition of error information is shown on page 125.

Error Information Example 1:

After establish a protected area with Set Max address, if a user attempts to change maximum LBA address (Device Configuration Set or Device Configuration Restore), device shall abort that command and return error reason code as below.

Cylinder high	:	03h	= word 3 is invalid
Cylinder low	:	00h	this register is not assigned in this case
Sector Number	:	00h	this register is not assigned in this case
Sector count	:	06h	= Protected area is now established

Error Information Example 2:

When device is enabled the Security feature set, if user attempts to disable that feature, device abort that command and return error reason code as below.

Cylinder high	:	07h	= word 7 is invalid
Cylinder low	:	00h	= bit 8-15 are valid
Sector Number	:	08h	= bit 3 is invalid
Sector count	:	04h	= now Security feature set is enabled

Word	Content	
0	0002h	Data Structure revision
1	Multiword DMA modes supported	
	15-3	Reserved
	2	1 = Multiword DMA mode 2 and below are supported
	1	1 = Multiword DMA mode 1 and below are supported
	0	1 = Multiword DMA mode 0 is supported
2	Ultra DMA modes supported	
	15-7	Reserved
	6	1 = Ultra DMA mode 6 and below are supported
	5	1 = Ultra DMA mode 5 and below are supported
	4	1 = Ultra DMA mode 4 and below are supported
	3	1 = Ultra DMA mode 3 and below are supported
	2	1 = Ultra DMA mode 2 and below are supported
	1	1 = Ultra DMA mode 1 and below are supported
	0	1 = Ultra DMA mode 0 is supported
3-6	Maximum LBA address	
7	Command set/feature set supported	
	15	0 = Reserved
	14	0 = Reserved
	13	0 = Reserved
	12	1 = SMART Selective self-test is supported
	11	1 = Forced Unit Access is supported
	10	0 = Reserved
	9	1 = Streaming feature set is supported
	8	1 = 48-bit Addressing feature set supported
	7	1 = Host Protected Area feature set supported
	6	1 = Automatic acoustic management supported
	5	1 = Read/Write DMA Queued commands supported
	4	1 = Power-up in Standby feature set supported
	3	1 = Security feature set supported
	2	1 = SMART error log supported
	1	1 = SMART self-test supported
	0	1 = SMART feature set supported
8	Serial ATA command / feature sets supported	
	15-5	Reserved
	4	1 = Supports software settings preservation
	3	Reserved
	2	1 = Supports interface power management
	1	1 = Supports non-zero buffer offset in DMA Setup FIS
	0	1 = Supports native command queuing
9-20	Reserved	
21	15-14	Reserved
	13	1 = Support for WRITE UNCORRECTABLE is allowed
	12-0	Reserved
22-254	Reserved	
255	Integrity word <Note .>	
	15-8	Checksum
	7-0	Signature (A5h)

Table 86 Device Configuration Overlay Data structure

Note.

Bits 7:0 of this word contain the value A5h. Bits 15:8 of this word contain the data structure checksum. The data

structure checksum is the two's complement of the sum of all byte in words 0 through 254 and the byte consisting of bits 7:0 of word 255. Each byte is added with unsigned arithmetic, and overflow is ignored. The sum of all bytes is zero when the checksum is correct.

Cylinder high	invalid word location	
Cylinder low	invalid bit location (bits (15:8))	
Sector number	invalid bit location (bits (7:0))	
Sector count	error reason code & description	
	01h	DCO feature is frozen
	02h	Device is now Security Locked mode
	03h	Device's feature is already modified with DCO
	04h	User attempt to disable any feature enabled
	05h	Device is now SET MAX Locked or Frozen mode
	06h	Protected area is now established
	07h	DCO is not supported
	08h	Subcommand code is invalid
	FFh	other reason

Table 87 DCO error information definition

10.5 Download Microcode (92h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	SUBCOMMAND(00-07)							
Sector Count	SECTOR_COUNT(00-07)							
Sector Number	SECTOR_COUNT(08-15)							
Cylinder Low	BUFFER_OFFSET(00-07)							
Cylinder High	BUFFER_OFFSET(08-15)							
Device/Head	-	-	-	D	-	-	-	-
Command	1	0	0	1	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	1	0	1	0	0	-	V

Table 88 Download Microcode Command (92h)

Output Parameters To The Device

Feature Subcommand code.

03h : Download and save microcode with offsets.

07h : Download and save microcode.

Other values are reserved.

Sector Count Lower byte of 16-bit sector count value to transfer from the host.

Sector Number Higher byte of 16-bit sector count value to transfer from the host.

Cylinder Buffer offset (only used for Feature = 03h)

This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE commands is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the Sector Number and Sector Count registers. The Sector Number register is used to extend the Sector Count register to create a 16-bit sector count value. The Sector Number register is the most significant eight bits and the Sector Count register is the least significant eight bits. A value of zero in both the Sector Number and Sector Count registers shall indicate no data is to be transferred.

ABT will be set to 1 in the Error Register if the value in the Feature register is neither 03h nor 07h, or the device is in Security Locked mode. When the reload of new microcode is requested in the data sent by the host for this Download command, UNC error will be set to 1 in the Error Register if the device fails to reload new microcode. This error is reported only when the reload of microcode is requested.

In reloading new microcode, when the spin-up of the device is disabled, the device spins down after reloading new microcode.

A Features register value of 03h indicates that the microcode will be transferred in two or more Download Microcode commands using the offset transfer method. The buffer offset value is defined by the value in Cylinder registers. The buffer offset value is the starting location in the microcode file, which varies in 512 byte increments.

All microcode segments shall be sent to the device in sequence.

The device may abort the DOWNLOAD MICROCODE command and discard all previously downloaded Microcode, if the current buffer offset is not equal to the sum of the previous DOWNLOAD MICROCODE command buffer offset and the previous sector count. The first DOWNLOAD MICROCODE command shall have a buffer offset of zero.
The new firmware should become effective immediately after the transfer of the last data segment has completed.

When the device detects the last download microcode command for the firmware download the device shall perform any device required verification and save the complete set of downloaded microcode.

If the device receives a command other than download microcode prior to the receipt of the last segment the new command is executed and all previously downloaded microcode is discarded.

If a software or hardware Reset is issued to the device before all of the microcode segments have been transferred to the device the device shall abandon all of the microcode segments received and process the Reset.

10.6 Execute Device Diagnostic (90h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	-	-	-	-	-
Command	1	0	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register
Diagnostic Code

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	0

Table 89 Execute Device Diagnostic Command (90h)

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code, refer to Error Register Diagnostic codes in Table 48 on page 65 for its definition.

10.7 Flush Cache (E7h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 90 Flush Cache Command (E7h)

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to disk media.

10.8 Flush Cache Ext (EAh)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		-	-	-	D	-	-	-	-
Command		1	1	1	0	1	0	1	0

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 91 Flush Cache Ext Command (EAh)

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to disk media.

10.9 Format Track (50h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	1	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 92 Format Track Command(50h)

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with write operation. At this time, whether the sector of data is initialized correctly is not verified with read operation. Any data previously stored on the track will be lost.

The host may transfer a sector of data containing a format table to the device. But the device ignores the format table and writes zero to all sectors on the track regardless of the descriptors.

Since device performance is optimal at 1:1 interleave, and the device uses relative block addressing internally, the device will always format a track in the same way no matter what sector numbering is specified in the format table.

Output Parameters To The Device

Sector Number	In LBA mode, this register specifies LBA address bits 0 - 7 to be formatted. (L=1)
Cylinder High/Low	The cylinder number of the track to be formatted. (L=0) In LBA mode, this register specifies LBA address bits 8-15 (Low), 16-23 (High) to be formatted. (L=1)
H	The head number of the track to be formatted. (L=0) In LBA mode, this register specifies LBA address bits 24-27 to be formatted. (L=1)

Input Parameters From The Device

Sector Number	In LBA mode, this register specifies current LBA address bits 0-7. (L=1)
Cylinder High/Low	In LBA mode, this register specifies current LBA address bits 8-15 (Low), 16-23 (High)
H	In LBA mode, this register specifies current LBA address bits 24-27. (L=1)
Error	The Error Register. An Abort error (ABT=1) will be returned when LBA out of range.

In LBA mode, this command formats a single logical track including the specified LBA.

10.10Format Unit (F7h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	0	0	1	0	0	0	1
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	L	1	D	-	-	-	-
Command	1	1	1	1	0	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	8	9	10	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	0	-	V

Table 93 Format Unit Command (F7h)

The Format Unit command initializes all user data sectors after merging reassigned sector location into the defect information of the device and clearing the reassign information. Both new reassign information and new defect information are available right after command completion of this command. Previous information of reassign and defect are erased from the device by executing this command.

Note that the Format Unit command initializes from LBA 0 to Native MAX LBA regardless of setting by Initialize Device Parameter (91h) command, Device Configuration Overlay, or Set Max Address (F9h) command, so the protected area defined by these commands is also initialized.

Security Erase Prepare (F3h) commands should be completed just prior to the Format Unit command. If the device receives a Format Unit command without a prior Security Erase Prepare command, the device aborts the Format Unit command.

All values in Feature register are reserved, and any values other than 11h should not be put into Feature register.

This command does not request to data transfer.

Command execution time depends on drive capacity. To determine command timeout value, Word 89 of Identify Device data should be referred.

10.11Identify Device (ECh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 94 Identify Device Command (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information described in the following pages.

Word	Content		Description
00	045AH or 045EH		Drive classification, bit assignments: 15 (=0): 1=ATAPI device, 0=ATA device 14 - 8 : retired 7 (=0): 1=removable cartridge device 6 (=1): 1=fixed device 5 - 3 : retired 2 (=0): Response incomplete 1 : retired 0 (=0): Reserved
01	xxxxH		Number of cylinders in default translate mode
02	C837H		Specific Configuration 37C8H: Need Set Feature for spin-up after power-up Identify Device is incomplete 738CH: Need Set Feature for spin-up after power-up Identify Device is complete 8C73H: No Need Set Feature for spin-up after power-up Identify Device is incomplete C837H: No Need Set Feature for spin-up after power-up Identify Device is complete
03	00xxH		Number of heads in default translate mode
04	0	*	Reserved
05	0	*	Reserved
06	003FH		Number of sectors per track in default translate mode
07	0000H	*	Number of bytes of sector gap
08	0000H	*	Number of bytes in sync field
09	0000H	*	Reserved
10-19	XXXX		Serial number in ASCII (0 = not specified)
20	0003H	*	Controller type: 0003: dual ported, multiple sector buffer with look-ahead read
21	XXXXH	*	Buffer size in 512-byte increments
22	0038H	*	Number of ECC bytes (Vendor unique length selected via set feature cmd)
23-26	XXXX		Microcode version in ASCII
27-46	XXXX		Model number in ASCII
47	8010H		15-8 : 80h 7-0 : Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands
48	4000H		Trusted Computing feature set options 15(=0) : Shall be cleared to zero 14(=1) : Shall be set to one 13-1(=0) : Reserved for the Trusted Computing Group 0(=0) : 0=Trusted Computing feature set is not supported

Table 95 Identify device information

Word	Content	Description
49	xF00H	Capabilities, bit assignments: 15-14 (=0) Reserved 13 Standby timer (=1) values as specified in ATA standard are supported (=0) values are vendor specific 12 (=0) Reserved 11 (=1) IORDY Supported 10 (=1) IORDY can be disabled 9 (=1) LBA supported 8 (=1) DMA supported 7- 0 (=0) Reserved
50	4000H	Capabilities, bit assignments: 15-14(=01) word 50 is valid 13- 1 (=0) Reserved 0 Minimum value of Standby timer (=0) less than 5 minutes
51	0200H	PIO data transfer cycle timing mode
52	0200H *	DMA data transfer cycle timing mode Refer Word 62 and 63
53	0007H	Validity flag of the word 15- 8(=0): Free-fall Control Sensitivity 00h = Vendor's recommended setting 7-3(=0): Reserved 2(=1): 1=Word 88 is Valid 1(=1): 1=Word 64-70 are Valid 0(=1): 1=Word 54-58 are Valid
54	xxxxH	Number of current cylinders
55	xxxxH	Number of current heads
56	xxxxH	Number of current sectors per track
57-58	xxxxH	Current capacity in sectors Word 57 specifies the low word of the capacity
59	0xxxH	Current Multiple setting. bit assignments 15- 9 (=0) Reserved 8 1= Multiple Sector Setting is Valid 7- 0 xxh = Current setting for number of sectors
60-61	xxxxH	Total Number of User Addressable Sectors Word 60 specifies the low word of the number FFFFFFFh=The 48-bit native max address is greater than 268,435,455
62	0000H	
63	xx07H	Multiword DMA Transfer Capability 15- 8 Multi word DMA transfer mode active 7- 0 (=7) Multi word DMA transfer modes supported (support mode 0,1 and 2)
64	0003H	Flow Control PIO Transfer Modes Supported 15-8(=0) Reserved 7-0 (=3) Advanced PIO Transfer Modes Supported '11' = PIO Mode 3 and 4 Supported
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15-0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)

Table 96 Identify device information --Continued--

Word	Content	Description
66	0078H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time
		15-0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
67	0078H	Minimum PIO Transfer Cycle Time Without Flow Control
		15-0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control
		15- 0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
69-74	0000H	Reserved
75	001FH	Queue depth
		15-5(=0) Reserved
		4-0(=1F) Maximum queued depth - 1
76	170xH	SATA capabilities
		15-13(=0) Reserved
		12(=1) High Priority command (Please see 6.5 First-party DMA commands)
		11(=0) Reserved
		10(=1) Phy event counters
		9(=1) Receipt of host-initiated interface power management requests
		8(=1) Native Command Queuing supported
		7-3(=0) Reserved
		2(=**x**) SATA Gen-2 speed (3.0Gbps) supported*
		1(=1) SATA Gen-1 speed (1.5Gbps) supported
		0(=0) Reserved
77	0000H	Reserved
78	005EH	SATA supported features
		15-7(=0) Reserved
		6(=1) Software setting preservation
		5(=0) Reserved
		4(=1) In-order data delivery
		3(=1) Device initiated interface power management
		2(=1) DMA Setup Auto-Activate optimization
		1(=1) Non-zero buffer offset in DMA Setup FIS
		0(=0) Reserved
79	0040H	SATA enabled features
		15-7(=0) Reserved
		6(=1) Software setting preservation
		5(=0) Reserved
		4(=0) In-order data delivery
		3(=0) Device initiated interface power management
		2(=0) DMA Setup Auto-Activate optimization
		1(=0) Non-zero buffer offset in DMA Setup FIS
		0(=0) Reserved
80	01FCH	Major version number
		15-0(=1FCh) ATA-2, ATA-3, ATA/ATAPI-4, ATA/ATAPI-5, ATA/ATAPI-6. ATA/ATAPI-7 and ATA8-ACS
81	0029H	Minor version number
		15-0(=29h) ATA8-ACS Revision 4

Table 97 Identify device information --Continued—

* 3.0Gbps is default setting; however, 1.5Gbps is supported.

Word	Content	Description
82	346BH	Command 15 (=0) Reserved 14 (=0) NOP command 13 (=1) READ BUFFER command 12 (=1) WRITE BUFFER command 11 (=0) Reserved 10 (=1) Host Protected Area Feature Set 9 (=0) DEVICE RESET command 8 (=0) SERVICE interrupt 7 (=0) Release interrupt 6 (=1) LOOK AHEAD 5 (=1) WRITE CACHE 4 (=0) PACKET Command feature set 3 (=1) Power management feature set 2 (=0) Removable feature set 1 (=1) Security feature set 0 (=1) SMART feature Set

Table 98 Identify device information --Continued--

Word	Content	Description
83	7FE9H	Command set supported 15-14(=01) Word 83 is valid 13 (=1) FLUSH CACHE EXT command supported 12 (=1) FLUSH CACHE command supported 11 (=1) Device Configuration Overlay command supported 10 (=1) 48-bit Address feature set supported 9 (=1) Automatic Acoustic Management 8 (=1) SET Max Security extension 7 (=1) Set Features Address Offset feature mode 6 (=1) SET FEATURES subcommand required to spin-up after power-up 5 (=1) Power-Up In Standby feature set supported 4 (=0) Removable Media Status Notification feature 3 (=1) Advanced Power Management feature set 2 (=0) CFA feature set 1 (=0) READ/WRITE DMA QUEUED 0 (=1) DOWNLOAD MICROCODE command
84	4163H or 4773H	Command set/feature supported extension 15-14(=01) Word 84 is valid 13(=0) IDLE IMMEDIATE with UNLOAD FEATURE supported 12-11(= 0) Reserved 10 (=x) URG bit supported for WRITE STREAM DMA and WRITE STREAM PIO 9 (=x) URG bit supported for READ STREAM DMA and READ STREAM PIO 8 (=1) World wide name supported 7 (=0) WRITE DMA QUEUED FUA EXT command supported 6 (=1) WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported 5 (=1) General Purpose Logging feature set supported 4 (=x) Streaming feature set supported 3 (=0) Media Card Pass Through Command feature set supported 2 (=0) Media serial number supported 1 (=1) SMART self-test supported 0 (=1) SMART error logging supported
85	xxxxH	Command set/feature enabled 15 Reserved 14 NOP command 13 READ BUFFER command 12 WRITE BUFFER command 11 Reserved 10 Host Protected Area feature set 9 DEVICE RESET command 8 SERVICE interrupt 7 RELEASE interrupt 6 LOOK AHEAD 5 WRITE CACHE 4 PACKET Command feature set 3 Power management feature set 2 Removable media feature set 1 Security feature set 0 SMART feature set

Table 99 Identify device information --Continued--

Word	Content	Description
86	xxxxH	Command set/feature enabled 15 Words 120:119 are valid. 14 Reserved 13 FLUSH CACHE EXT command supported 12 FLUSH CACHE command supported 11 Device Configuration Overlay command enabled 10 48-bit Address features set supported 9 Automatic Acoustic Management enabled 8 Set Max Security extensions enabled 7 Set Features Address Offset mode 6 Set Features subcommand required to spin-up after power-up 5 Power-Up In Standby feature set enabled 4 Removable Media Status Notification feature 3 Advanced Power Management Feature set 2 CFA Feature set 1 READ/WRITE DMA QUEUED 0 DOWNLOAD MICROCODE command
87	4163H or 4763H or 4773H	Command set/feature default 15-14(=01) Word 87 is valid 13(=0) IDLE IMMEDIATE with UNLOAD FEATURE supported 12-11(= 0) Reserved 10 (=x) URG bit supported for WRITE STREAM DMA and WRITE STREAM PIO 9 (=x) URG bit supported for READ STREAM DMA and READ STREAM PIO 8 (=1) World wide name supported 7 (=0) WRITE DMA QUEUED FUA EXT command supported 6 (=1) WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported 5 (=1) General Purpose Logging feature set supported 4 (=x) Valid CONFIGURE STREAM command has been executed 3 (=0) Media Card Pass Through Command feature set enabled 2 (=0) Media serial number is valid 1 (=1) SMART self-test supported 0 (=1) SMART error logging supported

Table 100 Identify device information --Continued--

Word	Content	Description
88	0x7FH	Ultra DMA Transfer modes 15- 8(=xx) Current active Ultra DMA transfer mode 15 Reserved (=0) 14 Mode 6 1 = Active 0 = Not Active 13 Mode 5 1 = Active 0 = Not Active 12 Mode 4 1 = Active 0 = Not Active 11 Mode 3 1 = Active 0 = Not Active 10 Mode 2 1 = Active 0 = Not Active 9 Mode 1 1 = Active 0 = Not Active 8 Mode 0 1 = Active 0 = Not Active 7- 0(=7F) Ultra DMA transfer mode supported 7 Reserved (=0) 6 Mode 6 1 = Support 5 Mode 5 1 = Support 4 Mode 4 1 = Support 3 Mode 3 1 = Support 2 Mode 2 1 = Support 1 Mode 1 1 = Support 0 Mode 0 1 = Support
89	xxxxH	Time required for security erase unit completion Time= value(xxxxh)*2 [minutes]
90	0000H	Time required for Enhanced security erase completion
91	0000H	Current Advanced power management value
92	FFFEH	Current Password Revision Code
93	0000H	COMRESET result

Table 101 Identify device information --Continued--

Word	Content	Description
94	xxxxH	Current Automatic Acoustic Management value 15-8 Vendor's Recommended Acoustic Management level 7-0 Current Automatic Acoustic Management value
95	xxxxH	Stream Minimum Request Size Number of sectors that provides optimum performance in streaming environment. This number shall be a power of two, with a minimum of eight sectors (4096 bytes). The starting LBA value for each streaming command should be evenly divisible by this request size.
96	xxxxH	Streaming Transfer Time - DMA The worst-case sustainable transfer time per sector for the device is calculated as follows: Streaming Transfer Time = (word 96) * (words(99:98) / 65536) If the Streaming Feature set is not supported by the device, the content of word 96 shall be zero.
97	xxxxH	Streaming Access Latency - DMA and PIO The worst-case access latency of the devoce for a streaming command is calculated as follows: Access Latency = (word 97) * (words(99:98) / 256) If the Streaming Feature set is not supported by the device, the content of word 97 shall be zero.
98-99	xxxxH	Streaming Performance Granularity These words define the fixed unit of time that is used in Identify Device words (97:96) and (104),and Set Features subcommand 43h, and in the Streaming Performance Parameters log, which is accessed by use of the Read Log Ext command, and in the Command Completion Time Limit that is passed in streaming commands. The unit of time for this parameter shall be in microseconds, e.g. ad value of 10000 indicates 10 ms.
100-103	xxxxH	Maximum user LBA address for 48-bit Address feature set
104	xxxxH	Streaming Transfer Time - PIO The worst-case sustainable transfer time per sector for the device is calculated as follows: Streaming Transfer Time = (word 104) * (words(99:98) / 65536) If the Streaming Feature set is not supported by the device, the content of word 104 shall be zero.
105-106	0000H	Reserved
107	5A87H	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108-111	xxxxH	World wide name the optional value of the world wide name for the device
112-118	0000H	Reserved
119	4014h	Supported settings (Continued from word 84:82) 15 Shall be cleared to zero 14 Shall be set to one. 13-6 Reserved 5 0=Free-fall Control feature set is not supported 4 1=The segmented feature for download microcode is supported. 3 0=Read and Write DMA Ext GPL optional commands are not supported. 2 1=Write Uncorrectable is supported. 1 0=Write-Read-Verify feature set is not supported 0 Reserved
120	4014h	Command set/feature enabled/supported. (Continued from word 87:85) 15 Shall be cleared to zero 14 Shall be set to one. 13-6 Reserved 5 0=Free-fall Control feature set is disabled 4 1=The segmented feature for download microcode is supported. 3 0=Read and Write DMA Ext GPL optional commands are not supported. 2 1=Write Uncorrectable is supported. 1 0=Write-Read-Verify feature set is not enabled 0 Reserved
121-126	0000H	Reserved
127	0000H	Removable Media Status Notification feature set 0000H=Not supported

Table 102 Identify device information --Continued--

Word	Content		Description		
128	xxxxH		Security status. Bit assignments		
			15-9	Reserved	
			8	Security Level	1= Maximum, 0= High
			7-6	Reserved	
			5	Enhanced erase	1= Support
			4	Expired	1= Expired
			3	Freeze	1= Frozen
			2	Lock	1= Locked
			1	Enabled/Disable	1= Enable
			0	Capability	1= Support
129	xxxxH	*	Current Set Feature Option. Bit assignments		
			15-4	Reserved	
			3	Auto reassign enabled	1= Enable
			2	Reverting enabled	1= Enable
			1	Read Look-ahead enabled	1= Enable
			0	Write Cache enabled	1= Enable
130-159	xxxxH	*	Reserved		
160-175	0000H		Reserved		
176-205	0000H		Current media serial number (0000H=Not supported)		
206			SCT Command set support		
			15-12	Vendor specific	
			11-6	Reserved	
			5	Action Code 5 (SCT Data Table)	1= Support
			4	Action Code 4 (Features Control)	1= Support
			3	Action Code 3 (Error Recovery Control)	1= Support
			2	Action Code 2 (LBA Segment Access)	1= Support
			1	Action Code 1 (Long Sector Access)	0= Not Support
			0	SCT Feature Set (includes SCT status)	1= Support

Table 103 Identify device information --Continued--

Note. The '*' mark in 'Content' field indicates the use of those parameters are vendor specific.

Word	Content	Description
207-208	0000H	Reserved
209	0000H	Alignment of logical blocks within a larger physical block 0000H=Not supported
210-211	0000H	Write-Read-Verify Sector Count Mode 3 (DWord) 0000H=Not supported
212-213	0000H	Write-Read-Verify Sector Count Mode 2 (DWord) 0000H=Not supported
214	0000H	NV Cache Capabilities 0000H=Not supported
215-216	0000H	NV Cache Size in Logical Blocks (DWord)
217	1C20H	Nominal media rotation rate (=7200rpm)
218	0000H	Reserved
219	0000H	NV Cache Options 0000H=Not supported
220	0000H	15-8(=0) Reserved 7-0(=0) Write-Read-Verify feature set current mode(not supported)
221	0000H	Reserved
222	101FH	Transport major version number 15-12(=1) Transport Type (1= Serial) 11-5(=0) Reserved 4(=1) SATA Rev 2.6 3(=1) SATA Rev 2.5 2(=1) SATA II: Extensions 1(=1) SATA 1.0a 0(=1) ATA8-AST
223	0021H	Transport minor version number (ATA8-AST T13 Project D1697 Revision 0b)
224-233	0000H	Reserved
234	0001H	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 3
235	03E0H	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 3
223	0021H	Transport minor version number (ATA8-AST T13 Project D1697 Revision 0b)
255	xxA5H	15-8 Checksum. This value is the two's complement of the sum of all bytes in byte 0 through 510 7-0 (A5) Signature

Table 104 Identify device information --Continued--

10.12Idle (E3h/97h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 105 Idle Command (E3h/97h)

The Idle command causes the device to enter Idle mode immediately, and set auto power down timeout parameter (standby timer). And then the timer starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is shown below:

Value	Timeout
0	Timer disabled
1-240	Value * 5
241-251	(Value-240) * 30 minutes
252	21 minutes
253	8 hours
254	21 minutes 10 seconds
255	21 minutes 15 seconds

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

10.13Idle Immediate (E1h/95h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 106 Idle Immediate Command (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect to auto power down timeout parameter.

10.14Initialize Device Parameters (91h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 107 Initialize Device Parameters Command (91h)

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54-58 in Identify Device Information reflect these parameters.

The parameters remain in effect until following events:

- Another Initialize Device Parameters command is received.
- The device is powered off.
- Soft reset occurs and the Set Feature option of CCh is set instead of 66h.

Output Parameters To The Device

Sector Count The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

H The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

Note: The following conditions needs to be satisfied to avoid invalid number of cylinders beyond FFFFh.

(Total number of user addressable sectors)/((Sector Count)*(H+1)) = < FFFFh

The total number of user addressable sectors is described in Identify Device command.

10.15Read Buffer (E4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 108 Read Buffer Command (E4h)

The Read Buffer command transfers a sector of data from the sector buffer of device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

10.16Read DMA(C8h/C9h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 109 Read DMA Command (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0)
	In LBA mode, this register specifies LBA address bits 0-7 to be transferred. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0)
	In LBA mode, this register specifies LBA address bits 8-15 (Low) 16-23 (High) to be transferred. (L=1)
H	The head number of the first sector to be transferred. (L=0)
	In LBA mode, this register specifies LBA bits 24-27 to be transferred. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 0-7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0)
	In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.17Read DMA Ext (25h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	0	1	0	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	Vs	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 110 Read DMA Ext Command (25h)

The Read DMA command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count Current	The number of sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of sectors to be transferred high order, bits (15:8). If 0000h in the Sector Count register is specified, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0)
Sector Number Previous	LBA (31:24)
Cylinder Low Current	LBA (15:8)
Cylinder Low Previous	LBA (39:32)
Cylinder High Current	LBA (23:16)
Cylinder High Previous	LBA (47:40)

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24)of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8)of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32)of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16)of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40)of the address of the first unrecoverable error.

10.18Read FPDMA Queued (60h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		V	1	0	0	-	-	-	-
Command		0	1	1	0	0	0	0	0

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	Vs	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 111 Read FPDMA Queued Command (60h)

The Read FPDMA command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Feature Current	The number of sectors to be transferred low order, bits (7:0).
Feature Previous	The number of sectors to be transferred high order, bits (15:8).
Sector Count Current	.
TAG (bits 7-3)	The TAG value shall be assigned to be different from all other queued commands. The value shall not exceed the maximum queue depth specified by the Word 75 of the Identify Device information.
Sector Count Previous	
PRIO (bits 7)	The Priority (PRIO) value shall be assigned by the host based on the priority of the command issued. The device shall make a best effort to complete High priority requests in a more timely fashion than Normal priority requests. The Priority values are defined as follows: 0b Normal priority 1b High priority
Sector Number Current	LBA (7:0)
Sector Number Previous	LBA (31:24)
Cylinder Low Current	LBA (15:8)
Cylinder Low Previous	LBA (39:32)
Cylinder High Current	LBA (23:16)
Cylinder High Previous	LBA (47:40)
Device/Head	
FUA (bit 7)	When the FUA bit is set to 1, the requested data is always retrieved from the media regardless of whether the data are held in the sector buffer or not. When the FUA bit is set to 0, the data may be retrieved from the media or from the cached data left by previously processed Read or Write commands.

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24)of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8)of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32)of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16)of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40)of the address of the first unrecoverable error.

10.19Read Log Ext (2Fh)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	-	1	D	-	-	-	-
Command		0	0	1	0	1	1	1	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 112 Read Log Ext Command (2Fh)

This command returns the specified log to the host. The device shall interrupt for each DRQ block transferred.

Output Parameters To The Device

Feature	Log Address Specific
Sector Count Current	The number of sectors to be read from the specified log low order, bits (7:0). The log transferred by the drive shall start at the sector in the specified log at the specified offset, regardless of the sector count requested.
Sector Count Previous	The number of sectors to be read from the specified log high orders, bits (15:8).
Sector Number Current	The log to be returned as described in 0.
Cylinder Low Current	The first sector of the log to be read low order, bits (7:0).
Cylinder Low Previous	The first sector of the log to be read high order, bits (15:8).

Log address	Content	Feature set	Type
00h	Log directory	N/A	Read Only
03h	Extended Comprehensive SMART error log	SMART error logging	Read Only
06h	SMART self-test log	SMART self-test	See Note
07h	Extended SMART self-test log	SMART self-test	Read Only
10h	Command Error	Native Command Queuing	Read Only
11h	Phy Event Counters	Serial ATA	Read Only
20h	Streaming Performance log	Streaming	Read Only
21h	Write Stream Error log	Streaming	Read Only
22h	Read Stream Error log	Streaming	Read Only
80h-9Fh	Host vendor specific	SMART	Read/Write

Note: If log address 06h is accessed using the Read Log Ext or Write Log Ext commands, command abort shall be returned.

Note: Please see 8.20.3 about Phy Event Counter.

Table 113 Log Address Definition

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log sector shall also be included in the Comprehensive SMART self-test log sector with the 48-bit entries.

If the feature set associated with the log specified in the Sector Number register is not supported or enabled, or if the values in the Sector Count, Sector Number or Cylinder Low registers are invalid, the device shall return command aborted.

10.19.1 General Purpose Log Directory

Table 113 defines the 512 bytes that make up the General Purpose Log Directory.

Description	Bytes	Offset
General Purpose Logging Version	2	00h
Number of sectors in the log at log address 01h (7:0)	1	02h
Number of sectors in the log at log address 01h (15:8)	1	03h
Number of sectors in the log at log address 02h (7:0)	1	04h
Number of sectors in the log at log address 02h (15:8)	1	05h
...		
Number of sectors in the log at log address 20h (7:0)	1	40h
Number of sectors in the log at log address 20h (15:8)	1	41h
Number of sectors in the log at log address 21h (7:0)	1	42h
Number of sectors in the log at log address 21h (15:8)	1	43h
Number of sectors in the log at log address 22h (7:0)	1	44h
Number of sectors in the log at log address 22h (15:8)	1	45h
...		
Number of sectors in the log at log address 80h (7:0)	1	100h
Number of sectors in the log at log address 80h (15:8)	1	101h
...		
Number of sectors in the log at log address FFh (7:0)	1	1FEh
Number of sectors in the log at log address FFh (15:8)	1	1FFh
	512	

Table 114 General Purpose Log Directory

The value of the General Purpose Logging Version word shall be 0001h. A value of 0000h indicates that there is no General Purpose Log Directory.

The logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

10.19.2 Extended Comprehensive SMART Error log

Table 114 defines the format of each of the sectors that comprise the Extended Comprehensive SMART error log. Error log data structure shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or in valid addresses.

Description	Bytes	Offset
SMART error log version	1	00h
Reserved	1	01h
Error log index (7:0)	1	02h
Error log index (15:8)	1	03h
1st error log data structure	124	04h
2nd error log data structure	124	80h
3rd error log data structure	124	FCh
4th error log data structure	124	178h
Device error count	2	1F4h
Reserved	9	1F6h
Data structure checksum	1	1FFh
	512	

Table 115 Extended Comprehensive SMART Error Log

10.19.2.1 Error log version

The value of this version shall be 01h.

10.19.2.2 Error log index

This indicates the error log data structure representing the most recent error. If there have been no error log entries, it is cleared to 0. Valid values for the error log index are 0 to 4.

10.19.2.3 Extended Error log data structure

An error log data structure shall be presented for each of the last four errors reported by the device.
These error log data structure entries are viewed as a circular buffer. The fifth error shall create an error log structure that replaces the first error log data structure. The next error after that shall create an error log data structure that replaces the second error log structure, etc.
Unused error log data structures shall be filled with zeros.

Data format of each error log structure is shown below.

Description	Bytes	Offset
1st command data structure	18	00h
2nd command data structure	18	12h
3rd command data structure	18	24h
4th command data structure	18	36h
5th command data structure	18	48h
Error data structure	34	5Ah
	124	

Table 116 Extended Error log data structure

Command data structure: Data format of each command data structure is shown below.

Description	Bytes	Offset
Device Control register	1	00h
Features register (7:0) (see Note)	1	01h
Features register (15:8)	1	02h
Sector count register (7:0)	1	03h
Sector count register (15:8)	1	04h
Sector number register (7:0)	1	05h
Sector number register (15:8)	1	06h
Cylinder Low register (7:0)	1	07h
Cylinder Low register (15:8)	1	08h
Cylinder High register (7:0)	1	09h
Cylinder High register (15:8)	1	0Ah
Device/Head register	1	0Bh
Command register	1	0Ch
Reserved	1	0Dh
Timestamp (milliseconds from Power-on)	4	0Eh
	18	

Note: bits (7:0) refer to the most recently written contents of the register. Bits (15:8) refer to the contents of the register prior to the most recent write to the register.

Table 117 Command data structure

Error data structure: Data format of error data structure is shown below.

Description	Bytes	Offset
Reserved	1	00h
Error register	1	01h
Sector count register (7:0) (see Note)	1	02h
Sector count register (15:8) (see Note)	1	03h
Sector number register (7:0)	1	04h
Sector number register (15:8)	1	05h
Cylinder Low register (7:0)	1	06h
Cylinder Low register (15:8)	1	07h
Cylinder High register (7:0)	1	08h
Cylinder High register (15:8)	1	09h
Device/Head register	1	0Ah
Status register	1	0Bh
Extended error data (vendor specific)	19	0Ch
State	1	1Fh
Life timestamp (hours)	2	20h
	34	

Note: bits (7:0) refer to the contents if the register is read with bit 7 of the Device Control register cleared to zero. Bits (15:8) refer to the contents if the register is read with bit 7 of the Device Control register set to one.

Table 118 Error data structure

State shall contain a value indicating the state of the device when the command was issued to the device or the reset occurred as described below.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle
x4h	SMART Off-line or Self-test
x5h-xAh	Reserved
xBh-xFh	Vendor specific
	Note: The value of x is vendor specific.

10.19.2.4 Device error count

This field shall contain the total number of errors attributable to the device that have been reported by the device during the life of the device. This count shall not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the device or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached the count shall remain at the maximum value when additional errors are encountered and logged.

10.19.3 Extended Self-test log sector

Table 118 defines the format of each of the sectors that comprise the Extended SMART self-test log.

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log, defined in 7.42.6, “Self-test log data structure" on page 230 shall also be included in the Extended SMART self-test log with all 48-bit entries.

Description	Bytes	Offset
Self-test log data structure revision number	1	00h
Reserved	1	01h
Self-test descriptor index (7:0)	1	02h
Self-test descriptor index (15:8)	1	03h
Descriptor entry 1	26	04h
Descriptor entry 2	26	1Eh
...		
Descriptor entry 18	26	1D8h
Vendor specific	2	1F2h
Reserved	11	1F4h
Data structure checksum	1	1FFh
	512	

Table 119 Extended Self-test log data structure

These descriptor entries are viewed as a circular buffer. The nineteenth self-test shall create a descriptor entry that replaces descriptor entry 1. The next self-test after that shall create a descriptor entry that replaces descriptor entry 2, etc. All unused self-test descriptors shall be filled with zeros.

10.19.3.1 Self-test log data structure revision number

The value of this revision number shall be 01h.

10.19.3.2 Self-test descriptor index

This indicates the most recent self-test descriptor. If there have been no self-tests, this is set to zero. Valid values for the Self-test descriptor index are 0 to 18.

10.19.3.3 Extended Self-test log descriptor entry

The content of the self-test descriptor entry is shown below.

Description	Bytes	Offset
Self-test number	1	00h
Self-test execution status	1	01h
Power-on life timestamp in hours	2	02h
Self-test failure check point	1	04h
Failing LBA (7:0)	1	05h
Failing LBA (15:8)	1	06h
Failing LBA (23:16)	1	07h
Failing LBA (31:24)	1	08h
Failing LBA (39:32)	1	09h
Failing LBA (47:40)	1	0Ah
Vendor specific	15	0Bh
	26	

Table 120 Extended Self-test log descriptor entry

10.19.4 Command Error

Table 120 defines the format of the Command Error data structure.

Byte	7	6	5	4	3	2	1	0
0	NQ	Reserved		TAG				
1	Reserved							
2	Status							
3	Error							
4	Sector Number							
5	Cylinder Low							
6	Cylinder High							
7	Dev/Head							
8	Sector Number Previous							
9	Cylinder Low Previous							
10	Cylinder High Previous							
11	Reserved							
12	Sector Count							
13	Sector Count Previous							
14 - 255	Reserved							
256 – 510	Vendor Unique							
511	Data Structure Checksum							

Table 121 Command Error information

The TAG field (Byte 0 Bits 4-0) contains the tag number corresponding to a queued command if the NQ bit is cleared.
The NQ field (Byte 0 Bit 7) indicates whether the error condition was a result of a non-queued or not. If it is cleared the error information corresponds to a queued command specified by the tag number indicated in the TAG field.
The bytes 1 to 13 correspond to the contents of Shadow Register Block when the error was reported.
The Data Structure Checksum (Byte 511) contains the 2's complement of the sum of the first 511 bytes in the data structure. The sum of all 512 bytes of the data structure will be zero when the checksum is correct.

10.19.5 Read Stream Error log

Table 121 defines the format of the Read Stream Error log. Entries are placed into the Read Stream Error log only when the SE bit is set to one in the Status Register. The 512 bytes returned shall contain a maximum of 31 error entries. The Read Stream Error Count shall contain the total number of Read Stream Errors detected since the last successful completion of the Read Log Ext command with LBA Low register set to 22h. This error count may be greater than 31, but only the most recent 31 errors are represented by entries in the log. If the Read Stream Error Count reaches the maximum value that can be represented after the next error is detected the Read Stream Error Count shall remain at the maximum value. After successful completion of a Read Log Ext command with the LBA Low Register set to 22h, the Read Stream Error Log shall be reset to a power-on or hardware reset condition, with the Error Log Index and Read Stream Error Count cleared to zero. The Read Stream Error Log is not preserved across power cycles and hardware reset.

Description	Bytes	Offset
Structure Version	1	00h
Error Log Index	1	01h
Read Stream Error Log Count	2	02h
Reserved	12	04h
Read Stream Error Log Entry #1	16	10h
Read Stream Error Log Entry #2	16	20h
...		
Read Stream Error Log Entry #31	16	1F0h
	512	

Table 122 Read Stream Error Log

The Data Structure Version field shall contain a value of 02h indicating the second revision of the structure format.

The Read Stream Error Log Count field shall contain the number of uncorrected sector entries currently reportable to the host. This value may exceed 31.

The Error Log Index indicates the error log data structure representing the most recent error. Only values (31:1) are valid.

Table 122 defines the format of each entry in the Read Stream Error Log.

Description	Bytes	Offset
Feature Register Contents Value (current)	1	00h
Feature Register Contents Value (previous)	1	01h
Status Register Contents Value	1	02h
Error Register Contents Value	1	03h
LBA (7:0)	1	04h
LBA (15:8)	1	05h
LBA (23:16)	1	06h
LBA (31:24)	1	07h
LBA (39:32)	1	08h
LBA (47:40)	1	09h
Reserved	2	0A-0Bh
Sector Count (LSB)	1	0Ch
Sector Count (MSB)	1	0Dh
Reserved	2	0E-0Fh

Table 123 Stream Error Log entry

Byte (1:0) contains the contents of the Feature Register when the error occurred. This Value shall be set to 0FFFFh for s deferred write error.

Byte 2 contains the contents of the Status Register when the error occurred.

Byte 3 contains the contents of the Error Register when the error occurred.

Byte (9:4) indicates the starting LBA of the error.

Byte (13:12) indicate the length of the error. Therefore, each entry may describe a range of sectors at the given address and spanning the specified number of sectors.

10.19.6 Write Stream Error log

Table 123 defines the format of the Write Stream Error log. Entries are placed into the Write Stream Error log only when the SE bit is set to one in the Status Register. The 512 bytes returned shall contain a maximum of 31 error entries. The Write Stream Error Count shall contain the total number of Write Stream Errors detected since the last successful completion of the Read Log Ext command with LBA Low register set to 21h. This error count may be greater than 31, but only the most 31 errors are represented by entries in the log. If the Write Stream Error Count reaches the maximum value that can be represented after the next error is detected the Write Stream Error Count shall remain at the maximum value. After successful completion of a Read Log Ext command with the LBA Low Register set to 21h, the Write Stream Error Log shall be reset to a power-on or hardware reset condition, with the Error Log Index and Write Stream Error Count cleared to zero. The Write Stream Error Log is not reserved across power cycles and hardware reset.

Description	Bytes	Offset
Structure Version	1	00h
Error Log Index	1	01h
Write Stream Error Log Count	2	02h
Reserved	12	04h
Write Stream Error Log Entry #1	16	10h
Write Stream Error Log Entry #2	16	20h
...		
Write Stream Error Log Entry #31	16	1F0h
	512	

Table 124 Write Stream Error Log

The Data Structure Version field shall contain a value of 02h indicating the second revision of the structure format.

The Write Stream Error Log Count field shall contain the number of Write Stream command entries since the last power on, since this log was last read, or since hardware reset was executed.

The Error Log Index indicates the error log data structure representing the most recent error. Only values (31:0) are valid.

0 defines the format of each entry in the Error Log.

10.19.7 Streaming Performance log

Table 124 defines the format of the log returned by the Read Log Ext command, when the LBA Low register is 20h. This data set is referred to as the Streaming Performance Parameters log, the length of which (in sectors) is statically indicated in Read Log Ext log address 00h (Log Directory).

The host should base its calculations on the larger of its Typical Host Interface Sector Time and the device reported Sector Time values, and on the sum of the device reported Access Time values and any additional latency that only the host is aware of (e.g. host command overhead, etc.).

Description	Bytes
Stream Performance Parameters log version	2
K, Number of Regions in Sector Time Array	2
L, Number of Positions in Position Array	2
M, Number of Position-differences in Access Time Array	2
Sector Time Array	K*8
Position Array	L*8
Access Time Array	M*4
Reserved	

Table 125 Streaming Performance Parameters log

Description	Bytes
LBA of reference location (LBA(7:0)...LBA(47:40))	n-(n+5)
(Identify Device words (99:98))/65536 time units per sector at the reference location	(n+6)-(n+7)

Table 126 Sector Time Array Entry (Linearly Interpolated)

Description	Bytes
LBA of start of region (LBA(7:0)...LBA(47:40))	n-(n+5)
Position number in the range 0...32767	(n+6)-(n+7)

Table 127 Position Array Entry (Linearly Interpolated)

Description	Bytes
Difference in position from last stream access to new stream access	n-(n+1)
Time that may be required to begin access at new stream access position, in (Identify Device words (99:98))/256 time units	(n+2)-(n+3)

Table 128 Access Time Array Entry (Linearly Interpolated)

10.20 Read Multiple (C4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 129 Read Multiple Command (C4h)

The Read Multiple command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sector(s) command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

10.21Read Multiple Ext (29h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	0	1	0	0	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 130 Read Multiple Ext Command (29h)

The Read Multiple Ext command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sector(s) command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If 0000h is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

10.22Read Native Max Address (F8h)

Block Output Registers Command								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	L	1	D	-	-	-	-
Command	1	1	1	1	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 131 Read Native Max ADDRESS (F8h)

This command returns the native max LBA/CYL of HDD which is not affected by Set Max Address command.

The 48-bit native max address is greater than 268,435,455; the Read Native Max Address command shall return a value of 268,435,455.

Input Parameters From The Device

Sector Number In LBA mode, this register contains native max LBA bits 0-7. (L=1)
In CHS mode, this register contains native max sector number. (L=0)

Cylinder High/Low In LBA mode, this register contains native max LBA bits 8-15 (Low), 16-23 (High). (L=1)
In CHS mode, this register contains native max cylinder number. (L=0)

H In LBA mode, this register contains native max LBA bits 24-27. (L=1)
In CHS mode, this register contains native max head number.(L=0)

10.23Read Native Max Address Ext (27h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	0	1	1	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 132 Read Native Max Address Ext (27h)

This command returns the native max LBA of HDD which is not effected by Set Max Address Ext command.

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the Native max address.
Sector Number (HOB=1)	LBA (31:24) of the address of the Native max address.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the Native max address.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the Native max address.
Cylinder High (HOB=0)	LBA (23:16) of the address of the Native max address.
Cylinder High (HOB=1)	LBA (47:40) of the address of the Native max address.

10.24Read Sector(s) (20h/21h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 133 Read Sector(s) Command (20h/21h)

The Read Sector(s) command reads one or more sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 – 27. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 – 27. (L=1)

10.25Read Sector(s) Ext (24h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	0	1	0	0

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 134 Read Sector(s) Ext Command (24h)

The Read Sector(s) Ext command reads from 1 to 65,536 sectors of data from disk media, and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

10.26Read Stream DMA (2Ah)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	-	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	1	0	1	0

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	CCTO
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	SE	DWE	DRQ	COR	IDX	ERR
0	V	V	0	-	0	-	V

Table 135 Read Stream DMA Command (2Ah)

The Read Stream DMA command reads one to 65536 sectors as specified in the Sector Count register. A value of 0000h in the Sector Count register requests 65536 sectors.

The RC bit indicates that the drive operate in a continuous read mode for the Read Stream command. When RC is cleared to zero the drive shall operate in normal Streaming read mode.

When the Read Continuous mode is enabled, the device shall transfer data of the requested length without setting the ERR bit to one. The SE bit shall be set to one if the data transferred includes errors. The data may be erroneous in this case.

If the Read Continuous bit is set to one, the device shall not stop execution of the command due to errors. If the RC bit is set to one and errors occur in reading or transfer of the data, the device shall continue to transfer the amount of data requested and then provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, ICRC,UNC,IDNF or ABRT, reported in the error log. If the RC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one, In all cases, the device shall attempt to transfer the amount of data requested within the Command Completion Time Limit event if some data transferred is in error.

Output Parameters To The Device

Feature Current

URG (bit7)	URG specifies an urgent transfer request. The Urgent bit specifies that the command should be completed in the minimum possible time by the device and shall be completed within the specified Command Completion Time Limit.
RC (bit6)	RC specifies Read Continuous mode enabled. If the Read Continuous bit is set to one, the device shall not stop execution of the command due to errors. If the RC bit is set to one and errors occur in reading or transfer of the data, the device shall continue to transfer the amount of data requested and then provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, ICRC, UNC, IDNF or ABRT reported in the error log. If the RC bit is set to one and the CCTL expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the CCTL expired by setting the CCTO bit in the error log to one. In all cases, the device shall attempt to transfer the amount of data requested within the CCTL even if some data transferred is in error.
NS (bit5)	NS (Not Sequential) may be set to one if the next read stream command with the same Stream ID may not be sequential in LBA space.
HSE (bit4)	HSE (Handle Stream Error) specifies that this command starts at the LBA of the last reported error for this stream, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier.
Stream ID (bit 0..2)	Stream ID specifies the stream to be read. The device shall operate according to the Stream ID set by the Read Stream command.
Feature Previous CCTL (7:0)	The time allowed for the current command's completion is calculated as follows: Command Completion Time Limit = (content of the Feature register Previous) * (Identify Device words (99:98)) useconds If the value is zero, the device shall use the Default CCTL supplied with a previous Configure Stream command for this Stream ID. If the Default CCTL is zero, or no previous Configure Stream command was defined for this Stream ID, the drive will ignore the CCTL. The time is measured from the write of the command register to the final INTRQ for command completion. The minimum CCTL is 50ms.CCTL is set to 50ms when the specified value is shorter than 50ms.
Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.
CCTO (Error, bit 0)	CCTO bit shall be set to one if a Command Completion Time Limit Out error has occurred.

SE (Status, bit 5)

SE (Stream Error) shall be set to one if an error has occurred during the execution of the command and the RC bit is set to one, In this case the LBA returned in the Sector Number registers shall be the address of the first sector in error, and the Sector Count registers shall contain the number of consecutive sectors that may contain errors. If the RC bit is set to one when the command is issued and ICRC, UNC, IDNF, ABRT, or CCTO error occurs, the SE bit shall be set to one, the ERR bit shall be cleared to zero, and the bits that would normally be set in the Error register shall be set in the error log.

10.27Read Stream PIO (2Bh)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	-	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	1	0	1	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	CCTO
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	SE	DWE	DRQ	COR	IDX	ERR
0	V	V	0	-	0	-	V

Table 136 Read Stream PIO Command (2Bh)

The Read Stream DMA command reads one to 65536 sectors as specified in the Sector Count register. A value of 0000h in the Sector Count register requests 65536 sectors.

The RC bit indicates that the drive operate in a continuous read mode for the Read Stream command. When RC is cleared to zero the drive shall operate in normal Streaming read mode.

When the Read Continuous mode is enabled, the device shall transfer data of the requested length without setting the ERR bit. The SE bit shall be set to one if the data transferred includes errors. The data may be erroneous in this case.

If the Read Continuous bit is set to one, the device shall not stop execution of the command due to errors. If the RC bit is set to one and errors occur in reading or transfer of the data, the device shall continue to transfer the amount of data requested and then provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, ICRC,UNC,IDNF, or ABRT, reported in the error log. If the RC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one, In all cases, the device shall attempt to transfer the amount of data requested within the Command Completion Time Limit event if some data transferred is in error.

Output Parameters To The Device

Feature Current

URG (bit7) URG specifies an urgent transfer request. The Urgent bit specifies that the command should be completed in the minimum possible time by the device and shall be completed within the specified Command Completion Time Limit.

RC (bit6)	RC specifies Read Continuous mode enabled. If the Read Continuous bit is set to one, the device shall not stop execution of the command due to errors. If the RC bit is set to one and errors occur in reading or transfer of the data, the device shall continue to transfer the amount of data requested and then provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, UNC, IDNF or ABRT reported in the error log. If the RC bit is set to one and the CCTL expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the CCTL expired by setting the CCTO bit in the error log to one. In all cases, the device shall attempt to transfer the amount of data requested within the CCTL even if some data transferred is in error.
NS (bit5)	NS (Not Sequential) may be set to one if the next read stream command with the same Stream ID may not be sequential in LBA space.
HSE (bit4)	HSE (Handle Stream Error) specifies that this command starts at the LBA of the last reported error for this stream, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier.
Stream ID (bit 0..2)	Stream ID specifies the stream to be read. The device shall operate according to the Stream ID set by the Read Stream command.
Feature Previous CCTL (7:0)	The time allowed for the current command's completion is calculated as follows: Command Completion Time Limit = (content of the Feature register Previous) * (Identify Device words (99:98)) microseconds If the value is zero, the device shall use the Default CCTL supplied with a previous Configure Stream command for this Stream ID. If the Default CCTL is zero, or no previous Configure Stream command was defined for this Stream ID, the device will ignore the CCTL. The time is measured from the write of the command register to command completion. The minimum CCTL is 50ms.CCTL is set to 50ms when the specified value is shorter than 50ms.
Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.
CCTO (Error, bit 0)	CCTO bit shall be set to one if a Command Completion Time Limit Out error has occurred.
SE (Status, bit 5)	SE (Stream Error) shall be set to one if an error has occurred during the execution of the command and the RC bit is set to one. In this case the LBA returned in the Sector Number registers shall be the address of the first sector in error, and the Sector Count registers shall contain the number of consecutive sectors that may contain errors. If the RC bit is set to one when the command is issued and a UNC, IDNF, ABRT, or CCTO error occurs, the SE bit shall be set to one, the ERR bit shall be cleared to zero, and the bits that would normally be set in the Error register shall be set in the error log.

10.28Read Verify Sector(s) (40h/41h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 137 Read Verify Sector(s) Command (40h/41h)

The Read Verify Sector(s) verifies one or more sectors on the device. No data is transferred to the host.

The difference between Read Sector(s) command and Read Verify Sector(s) command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 – 27. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 – 27. (L=1)

10.29Read Verify Sector(s) Ext (42h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	0	0	0	1	0

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 138 Read Verify Sector(s) Ext Command (42h)

The Read Verify Sector(s) Ext verifies one or more sectors on the device. No data is transferred to the host.

The difference between the Read Sector(s) Ext command and the Read Verify Sector(s) Ext command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the Read Verify Sector(s) Ext will be terminated at the failing sector.

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be verified low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be verified high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be verified.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24)
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

10.30 Recalibrate (1xh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	0	0	0	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 139 Recalibrate Command (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.
If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

10.31 Security Disable Password (F6h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 140 Security Disable Password Command (F6h)

The Security Disable Password command disables the security mode feature (device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in Table 139. Then the device checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be re-activated later by setting User Password. This command should be executed in device unlock mode.

Word	Description
00	Control word bit 0 : Identifier (1-Mater, 0-User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Table 141 Password Information for Security Disable Password command

The device will compare the password sent from this host with that specified in the control word.

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

10.32 Security Erase Prepare (F3h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 142 Security Erase Prepare Command (F3h)

The Security Erase Prepare Command must be issued immediately before the Security Erase Unit Command to enable device erasing and unlocking.

The Security Erase Prepare Command must be issued immediately before the Format Unit Command. This command is to prevent accidental erasure of the device.

This command does not request to transfer data.

10.33Security Erase Unit (F4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 143 Security Erase Unit Command (F4h)

The Security Erase Unit command initializes all user data sectors, and then disables the device lock function.

Note that the Security Erase Unit command initializes from LBA 0 to Native MAX LBA. Host MAX LBA set by Initialize Drive Parameter, Device Configuration Overlay, or Set MAX Address command is ignored. So the protected area by Set MAX Address command is also initialized.

This command requests to transfer a single sector data from the host including information specified in Table 143 on page 193.

If the password does not match, then the device rejects the command with an Aborted error.

Word	Description	
00	Control word	
	bit 0	: Identifier (1-Mater, 0-User)
	bit 1	: Erase mode (1- Enhanced, 0- Normal) Enhanced mode is not supported
	bit 2-15	: Reserved
01-16	Password	(32 bytes)
17-255	Reserved	

Table 144 Erase Unit Information

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

The Security Erase Unit command erases all user data and disables the security mode feature (device lock function). So after completing this command, all user data will be initialized to zero with write operation. At this time, it is not verified with read operation whether the sector of data is initialized correctly. Also, the defective sector information and the reassigned sector information for the device are not updated. The security erase prepare command should be completed immediately prior to the Security Erase Unit command. If the device receives a Security Erase Unit command without a prior Security Erase Prepare command, the device aborts the security erase unit command.

This command disables the security mode feature (device lock function), however the master password is still stored internally within the device and may be re-activated later when a new user password is set. If you execute this command on disabling the security mode feature (device lock function), the password sent by the host is NOT compared with the password stored in the device for both the Master Password and the User Password, and then the device only erases all user data.

The execution time of this command is set in word 89 of Identify device information.

10.34Security Freeze Lock (F5h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 145 Security Freeze Lock Command (F5h)

The Security Freeze Lock Command allows the device to enter frozen mode immediately.

After this command is completed, the command which updates Security Mode Feature (Device Lock Function) is rejected.

Frozen mode is quit only by Power off.

The following commands are rejected when the device is in frozen mode. For detail, refer to Table 50 on page 74 and 75.

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

10.35 Security Set Password (F1h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 146 Security Set Password Command (F1h)

The Security Set Password command enables security mode feature (device lock function), and sets the master password or the user password.

The security mode feature (device lock function) is enabled by this command, and the device is not locked immediately. The device is locked after next power on reset or hard reset. When the MASTER password is set by this command, the master password is registered internally, but the device is NOT locked after next power on reset or hard reset.

This command requests a transfer of a single sector of data from the host including the information specified in Table 146 on page 196.

The data transferred controls the function of this command.

Word	Description
00	Control word bit 0 : Identifier (1-Mater, 0-User) bit 1-7 : Reserved bit 8 : Security level (1-Maximum, 0-High) bit 9-15 : Reserved
01-16	Password (32 byte)
17	Master Password Revision Code (valid if Word 0 bit 0 = 1)
18-255	Reserved

Table 147 Security Set Password Information

Identifier Zero indicates that the device regards Password as User Password. One indicates that device regards Password as Master Password.

Security Level Zero indicates High level, one indicates Maximum level. If the host sets High level and the password is forgotten, then the Master Password can be used to unlock the device. If the host sets Maximum level and the user password is forgotten, only an Security Erase Prepare/Security Unit command can unlock the device and all data will be lost.

Password The text of the password – all 32 bytes are always significant.

Master Password Revision Code The revision code field is returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. The device accepts the command with a value of 0000h or FFFFh in this field, but does not change Master Password Revision code.

The setting of the Identifier and Security level bits interact as follows.

Identifier=User / Security level = High
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by either the user password or the previously set master password.

Identifier=Master / Security level = High
This combination will set a master password but will NOT enable the security mode feature (lock function).

Identifier=User / Security level = Maximum
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by only the user password. The master password previously set is still stored in the file but may NOT be used to unlock the device.

Identifier=Master / Security level = Maximum
This combination will set a master password but will NOT enable the security mode feature (lock function).

10.36 Security Unlock (F2h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 148 Security Unlock Command (F2h)

This command unlocks the password and causes the device to enter device unlock mode. If power on reset or hard reset is done without executing the Security Disable Password command after this command is completed, the device will be in device lock mode. The password has not been changed yet.

The Security Unlock command requests to transfer a single sector of data from the host including information specified in Table 148 on the page 198.

If the Identifier bit is set to master and the file is in high security mode then the password supplied will be compared with the stored master password. If the file is in maximum security mode then the security unlock will be rejected.

If the Identifier bit is set to user, then the file compares the supplied password with the stored user password.

If the password compare fails, then the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch.

When this counter reaches zero then all password protected commands are rejected until a hard reset or a power off.

Word	Description
00	Control word bit 0 : Identifier (1-Mater, 0-User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Table 149 Security Unlock Information

Identifier Zero indicates that device regards Password as User Password. One indicates that device regards Password as Master Password.

The user can detect if the attempt to unlock the device has failed due to a mismatched password as this is the only reason that an abort error will be returned by the file AFTER the password information has been sent to the device. If an abort error is returned by the device BEFORE the password data has been sent to the file then another problem exists.

10.37Seek (7xh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	1	1	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 150 Seek Command (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The device need not be formatted for a seek to execute properly.

Output Parameters To The Device

Sector Number In LBA mode, this register specifies LBA address bits 0 – 7 for seek. (L=1)

Cylinder High/Low The cylinder number of the seek.
In LBA mode, this register specifies LBA address bits 8 – 15 (Low), 16 – 23 (High) for seek. (L=1)

H The head number of the seek.
In LBA mode, this register specifies LBA address bits 24 – 27 for seek. (L=1)

Input Parameters From The Device

Sector Number In LBA mode, this register contains current LBA bits 0 – 7. (L=1)

Cylinder High/Low In LBA mode, this register contains current LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)

H In LBA mode, this register contains current LBA bits 24 – 27. (L=1)

10.38 Set Features (EFh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	Note.1							
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 151 Set Features Command (EFh)

The Set Feature command is to establish the following parameters which affect the execution of certain features as shown in below table.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

Output Parameters To The Device

Feature Destination code for this command

02H	Enable write cache
03H	Set transfer mode based on value in sector count register
05H	Enable Advanced Power Management
06H	Enable Power-up in Standby feature set
07H	Power-Up In Standby feature set device spin-up
09H	Enable Address Offset mode
10H	Enable use of Serial ATA feature
42H	Enable Automatic Acoustic Management
43H	Set Maximum Host Interface Sector Time
55H	Disable read look-ahead feature
66H	Disable reverting to power on defaults
82H	Disable write cache
85H	Disable Advanced Power Management
86H	Disable Power-up in Standby mode
89H	Disable Address Offset mode
90H	Disable use of Serial ATA feature
AAH	Enable read look-ahead feature
C2H	Disable Automatic Acoustic Management
CCH	Enable reverting to power on defaults

Note.

After power on reset or hard reset, the device is set to the following features as default.

Write cache	: Enable
Read look-ahead	: Enable
Reverting to power on defaults	: Disable
Release interrupt	: Disable

10.38.1 Set Transfer mode

When Feature register is 03h (=Set Transfer mode), the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000	000	
PIO Default Transfer Mode Disable IORDY	00000	001	
PIO Flow Control Transfer Mode x	00001	nnn	(nnn=000,001,010,011,100)
Multiword DMA mode x	00100	nnn	(nnn=000,001,010)
Ultra DMA mode x	01000	nnn	(nnn=000,001,010,011,100,101,110)

10.38.2 Write Cache

If the number of auto reassigned sector reaches the device's reassignment capacity, the write cache function will be automatically disabled. Although the device still accepts the Set Features command with Feature register = 02h without error, but the write cache function will remains disabled. For current write cache function status, please refer to Identify Device Information (word 85 or 129) by Identify Device command.

10.38.3 Serial ATA Feature

When the Feature register is set to 10h or 90h, the value set to the Sector Count register specifies the specific Serial ATA feature to enable or disable.

Sector Count Value	Description
01h	Non-zero buffer offset in DMA Setup FIS
02h	DMA Setup FIS Auto-Activate optimization
03h	Device-initiated interface power state transitions
04h	Guaranteed In-Order Data Delivery
06h	Software Settings Preservation

10.38.4 Advanced Power Management

When the value in the Feature register is 05h (=Enable Advanced Power Management), the Sector Count Register specifies the Advanced Power Management level.

FFh ---	Aborted
C0 – Feh ---	The deepest Power Saving mode is Normal Idle mode (the same as Disable Advanced Power Management)
80 – BFh ---	The deepest Power Saving mode is Low power Idle mode
01 – 7Fh ---	The deepest Power Saving mode is Low RPM standby mode
00h ---	Aborted

The idle time to Low power idle mode and Low RPM standby mode vary according to the value in Sector Count register as follows:

When Low power idle mode is the deepest Power Saving mode,

Y_1=(x-80h) * 5+120 [sec] (120<= Y_1<=435)

Y_2=N/A(the device does not go to Low RPM standby mode)

When Low RPM standby mode is the deepest Power Saving mode and the value in Sector Count register is between 40h and 7Fh,

120<=Y_1<=435 [sec] (default: 120 [sec])

Y_2=(x-40h) * 60 + 600[sec] (600<=Y_2<=4380)

When Low RPM standby mode is the deepest Power Saving mode and the value in Sector Count register is between 01h and 3Fh,

120<=Y_1<=435 [sec] (default: 120 [sec])

Y_2=600 [sec]

where x is the value in Sector Count register, y_1 is the idle time to Low Power Idle mode, and y_2 is the idle time to Low RPM standby mode.

If Low power idle mode has already been enabled (i.e., y_1 has been set) before Low RPM standby mode is enabled, y_1 is preserved. If Low power idle mode is disabled (i.e., y_1 has not been set yet), y_1 becomes 120[sec] when Low RPM standby mode is enabled.

Enabled Power Saving mode and idle time (y_1 and y_2) are preserved until Advanced Power Management is disabled, the deepest Power Saving mode becomes Normal Idle mode, or new time is set. They are initialized with a hard/soft reset unless Reverting to power on defaults is disabled and the device receives a soft reset.

10.38.4.1 Low Power Idle mode

Additional electronics are powered off, and heads are unloaded on the ramp, however the spindle is still rotated at the full speed.

10.38.4.2 Low RPM standby mode

The heads are unloaded on the ramp, and the spindle is rotated at the 60-65% of the full speed.

When Feature register is 85h (=Disable Advanced Power Management), the deepest Power Saving mode becomes normal Idle.

10.38.5 Automatic Acoustic Management

FF	---	Aborted
C0 – Feh	--	Set to Normal Seek mode
80 – BFh	---	Set to Quiet Seek mode
00 – 7Fh	---	Aborted

The device preserves enabling or disabling of Automatic Acoustic Management, and the current Automatic Acoustic Management level setting across all forms of reset, i.e., Power on, Hardware, and Software Resets.

10.38.6 Set Maximum Host Interface Sector Time

Sector Count	Typical PIO Mode Host Interface Sector Time (7:0)
LBA Low	Typical PIO Mode Host Interface Sector Time (15:8)
LBA Mid	Typical DMA Mode Host Interface Sector Time (7:0)
LBA High	Typical DMA Mode Host Interface Sector Time (15:8)

Subcommand code 43h allows the host to inform the device of a host interface rate limitation. The typical Host Interface Sector Times have the same units as Identify Device word 96 for DMA and word 104 for PIO. A value of zero indicates that the host interface shall be capable of transferring data at the maximum rate allowed by the selected transfer mode. The Typical PIO Mode Host Interface Sector Time includes the host's interrupt service time.

10.39 Set Max Address (F9h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	-	-	-	-	-	-	-	B
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	1	1	1	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 152 Set Max ADDRESS (F9h)

The device regards as Set Max Address command, if this command is immediately preceded by a Read Native Max Address command. The device receives this command without a prior Read Native Max Address command, the device regards as Set Max security extensions command according to feature register value. Valid features values are as follows:

1. 01h indicates Set Max Set Password command
2. 02h indicates Set Max Lock command
3. 03h indicates Set Max Unlock command
4. 04h indicates Set Max Freeze LOCK command

This command overwrites the maximum number of Address of HDD in a range of actual device capacity. Once device receives this command, all accesses beyond that Address are rejected with setting ABORT bit in status register. Identify device command returns the Address which is set via this command as a default value.

If the device in Address Offset mode receives this command with the nonvolatile option, the device returns aborted error to the host.

Device returns command aborted for a second non-volatile Set Max Address command until next power on or hardware reset.

Device returns command aborted during Set Max Locked mode or Set Max Frozen mode.

After a successful command completion, Identify Device response words (61:60) shall reflect the maximum address set with this command.

If the 48-bit Address feature set is supported, the value placed in Identify Device response words (103:100) shall be the same as the value placed in words (61:60). However, if the device contains greater than 268,435,455 sectors, the capacity addressable with 28-bit commands, and the address requested is 268,435,455, the max address shall be changed to the native maximum address, the value placed in words (61:60) shall be 268,435,455 and the value placed in words (103:100) shall be the native maximum address.

If a host protected area has been established by a Set Max Address Ext command, the device shall return command aborted.

Output Parameters To The Device

B	Option bit for selection whether nonvolatile or volatile. B=0 is volatile condition. When B=1, MAX Address which is set by Set Max Address command is preserved by POR. When B=0, MAX Address which is set by Set Max Address command will be lost by POR. B=1 is not valid when the device is in Address Offset mode.
Sector Number	In LBA mode, this register contains LBA bits 0 – 7 which is to be input.(L=1) In CHS mode, this register is ignored. (L=0)
Cylinder High/Low	In LBA mode, this register contains LBA bits 8 – 15 (Low), 16 – 23 (High) which is to be set. (L=1) In CHS mode, this register contains cylinder number which is to be set.(L=0)
H	In LBA mode, this register contains LBA bits 24 – 27 which is to be set.(L=1) In CHS mode, this register is ignored. (L=0)

Input Parameters From The Device

Sector Number	In LBA mode, this register contains max LBA bits 0 – 7 which is set.(L=1) In CHS mode, this register contains max sector number (= 63). (L=0)
Cylinder High/Low	In LBA mode, this register contains max LBA bits 8 – 15 (Low), 16 – 23 (High) which is set. (L=1) In CHS mode, this register contains max cylinder number which is set. (L=0)
H	In LBA mode, this register contains max LBA bits 24 – 27 which is set. (L=1) In CHS mode, this register contains max head number.(L=0)

10.39.1 Set Max Set Password (Feature = 01h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	0	0	0	0	0	0	1
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	1	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 153 Set Max set Password

The device regards as Set Max Address command, if this command is immediately preceded by a Read Native Max Address command.

This command requests a transfer of a single sector of data from the host including the information specified in Table 153.

The password is retained by the device until the next power cycle. When the device accepts this command the device is in Set_Max_Unlocked state.

Word	Description
0	Reserved
01-16	Password (32 byte)
17-255	Reserved

Table 154 Set Max Set Password data contents

10.39.2 Set Max Lock (Feature = 02h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	0	0	0	0	0	1	0
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	1	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 155 Set Max Lock

The device regards as Set Max Address command, if this command is immediately preceded by a Read Native Max Address command.

This command sets the device into Set_Max_Locked state. After this command is completed any other Set Max commands except Set Max Unlock and Set Max Freeze Lock are rejected. The device remains in this state until a power cycle or the acceptance of a Set Max Unlock or Set Max Freeze Lock command.

10.39.3 Set Max Unlock (Feature = 03h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	0	0	0	0	0	1	1
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	1	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 156 Set Max Unlock (F9h)

The device regards as Set Max Address command, if this command is immediately preceded by a Read Native Max Address command.

This command requests a transfer of a single sector of data from the host including the information specified in Table 153 on the page 207 with the stored SET MAX password.

If the password compare fails then the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch. When this counter reaches zero then all Set Max Unlock commands are rejected until a hard reset or a power off.

If the password compares matches, then the device set the Set_Max_Unlocked state and all Set Max commands shall be accepted.

10.39.4 Set Max Freeze Lock (Feature = 04h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	0	0	0	0	1	0	0
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	1	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 157 Set Max Freeze Lock (F9h)

The device regards as Set Max Address command, if this command is immediately preceded by a Read Native Max Address command.

The Set Max Freeze Lock command sets the device to Set_Max_Frozen state. After command completion any subsequent Set Max commands are rejected. Commands disabled by Set Max Freeze Lock are:

1. Set Max Address
2. Set Max Set PASSWORD
3. Set Max Lock
4. Set Max Unlock

10.40 Set Max Address Ext (37h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	-	-	-	-	-	-	-	B
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	0	1	1	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 158 Set Max Address Ext Command (37h)

This command is immediately preceded by a Read Native Max Address Ext command.

This command overwrites the maximum number of Address of HDD in a range of actual device capacity. Once device receives this command, all accesses beyond that Address are rejected with setting ABORT bit in status register.

When the address requested is greater than 268,435,455, words (103:100) shall be modified to reflect the requested value, but words (61:60) shall not be modified. When the address requested is equal to or less than 268,435,455, words (103:100) shall be modified to reflect the requested value, and words (61:60) shall also be modified.

If this command is not supported, the maximum value to be set exceeds the capacity of the device, a host protected area has been established by a Set Max Address command, the command is not immediately preceded by a Read Native Max Address Ext command, or the device is in the Set Max Locked or Set Max Frozen state, the device shall return command aborted.

If the device in Address Offset mode receives this command with the nonvolatile option, the device returns aborted error to the host.

The device returns the command aborted for a second non-volatile Set Max Address Ext command until next power on or hardware reset.

Output Parameters To The Device

B	Option bit for selection whether nonvolatile or volatile. B=0 is volatile condition. When B=1, MAX Address which is set by Set Max Address Ext command is preserved by POR. When B=0, MAX Address which is set by Set Max Address Ext command will be lost by POR. B=1 is not valid when the device is in Address Offset mode.
Sector Number Current	Set Max LBA (7:0).
Sector Number Previous	Set Max LBA (31:24).
Cylinder Low Current	Set Max LBA (15:8).
Cylinder Low Previous	Set Max LBA (39:32).
Cylinder High Current	Set Max LBA (23:16).
Cylinder High Previous	Set Max LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	Set Max LBA (7:0).
Sector Number (HOB=1)	Set Max LBA (31:24).
Cylinder Low (HOB=0)	Set Max LBA (15:8).
Cylinder Low (HOB=1)	Set Max LBA (39:32).
Cylinder High (HOB=0)	Set Max LBA (23:16).
Cylinder High (HOB=1)	Set Max LBA (47:40).

10.41Set Multiple (C6h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	0	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 159 Set Multiple Command (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Device

Sector Count. The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 1, 2, 4, 8 or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

10.42 Sleep (E6h/99h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 160 Sleep Command (E6h/99h)

This command causes the device to enter Sleep Mode.

The device is spun down and the interface becomes inactive. If the device is already spun down, the spin down sequence is not executed.

The only way to recover from Sleep Mode is with a software reset or a hardware reset.

10.43SMART Function Set (B0h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	0	1	0	0	1	1	1	1
Cylinder High	1	1	0	0	0	0	1	0
Device/Head	1	-	1	D	-	-	-	-
Command	1	0	1	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 161 SMART Function Set Command (B0h)

The SMART Function Set command provides access to Attribute Values, Attribute Thresholds and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The SMART Function Set command has several separate subcommands which are selectable via the device's Features Register when the SMART Function Set command is issued by the host.

10.43.1 SMART Subcommand

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands and their respective codes are listed below.

Code	Subcommand
D0h	SMART Read Attribute Values
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/disable Attribute Autosave
D3h	SMART Save Attribute Values
D4h	SMART Execute Off-line Immediate
D5h	SMART Read Log Sector
D6h	SMART Write Log Sector
D8h	SMART Enable Operations
D9h	SMART Disable Operations
Dah	SMART Return Status
DBh	SMART Enable/Disable Automatic Off-Line

10.43.1.1 SMART Read Attribute Values (Subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the SMART Read Attribute Values subcommand from the host, the device saves any updated Attribute Values to the Attribute Data sectors, and then transfers the 512 bytes of Attribute Value information to the host.

10.43.1.2 SMART Read Attribute Thresholds (Subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the SMART Read Attribute Thresholds subcommand from the host, the device reads the Attribute Thresholds from the Attribute Threshold sectors, and then transfers the 512 bytes of Attribute Thresholds information to the host.

10.43.1.3 SMART Enable/Disable Attribute Autosave (Subcommand D2h)

This subcommand enables and disables the attribute autosave feature of the device. The SMART Enable/Disable Attribute Autosave subcommand either allows the device to automatically save its updated Attribute Values to the Attribute Data Sector periodically; or this subcommand causes the autosave feature to be disabled. The state of the Attribute Autosave feature (either enabled or disabled) will be preserved by the device across power cycle.

A value of 00h written by the host into the device's Sector Count Register before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or power-down.

A value of F1h written by the host into the device's Sector Count Register before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing the SMART Enable/Disable Attribute Autosave subcommand will not change the current Autosave status but the device will respond with the error code specified in 0.

The SMART Disable Operations subcommand disables the autosave feature along with the device's SMART operations.

Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Autosave feature, clears BSY and asserts INTRQ.

10.43.1.4 SMART Save Attribute Values (Subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the SMART Save Attribute Values subcommand from the host, the device writes any updated Attribute Values to the Attribute Data sector.

10.43.1.5 SMART Execute Off-line Immediate (Subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an off-line mode (off-line routine) or execute a self-test routine in either captive or off-line mode.

The Sector Number register shall be set to specify the operation to be executed.

Sector Number	Operation to be executed
0	Execute SMART off-line data collection routine immediately
1	Execute SMART Short self-test routine immediately in off-line mode
2	Execute SMART Extended self-test routine immediately in off-line mode
4	Execute SMART Selective self-test routine immediately in off-line mode
127	Abort off-line mode self-test routine
129	Execute SMART Short self-test routine immediately in captive mode
130	Execute SMART Extended self-test routine immediately in captive mode
132	Execute SMART Selective self-test routine immediately in captive mode

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte (Table 162) and ATA registers as below and executes command completion.

Status	Set ERR to one when self-test has failed
Error	Set ABRT to one when self-test has failed
Cyl Low	Set to F4h when self-test has failed
Cyl High	Set to 2Ch when self-test has failed

10.43.1.6 SMART Read Log Sector (Subcommand D5h)

This command returns the specified log sector contents to the host.

The 512 bytes data are returned at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address.

Log sector address	Content	Type
00h	Log directory	Read Only
01h	Summary SMART Error Log	Read Only
03h	Extended Comprehensive SMART Error Log	See Note
06h	SMART Self-test Log	Read Only
07h	Extended Self-test Log	See Note
09h	Selective self-test Log	Read/Write
80h-9Fh	Host vendor specific	Read/Write

Note: Log addresses 03h and 07h are used by the Read Log Ext and Write Log Ext commands. If these log addresses are used with the SMART Read Log Sector command, the device shall return command aborted.

Table 162 Log sector addresses

10.43.1.7 SMART Write Log Sector (Subcommand D6h)

This command writes 512 bytes data to the specified log sector.

The 512 bytes data are transferred at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address (0). If Read Only log sector is specified, the device returns ABRT error

10.43.1.8 SMART Enable Operations (Subcommand D8h)

This subcommand enables access to all SMART capabilities within the device. Prior to receipt of a SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the SMART Enable Operations subcommand from the host, the device enables SMART capabilities and functions, and then saves any updated Attribute Values to the Attribute Data sector.

10.43.1.9 SMART Disable Operations (Subcommand D9h)

This subcommand disables all SMART capabilities within the device including the device's attribute autosave feature. After receipt of this subcommand the device disables all SMART operations. Non self-preserved Attribute Values will no longer be monitored. The state of SMART (either enabled or disabled) is preserved by the device across power cycles.

Upon receipt of the SMART Disable Operations subcommand from the host, the device disables SMART capabilities and functions, and then saves any updated Attribute Values to the Attribute Data sector.

After receipt of the device of the SMART Disable Operations subcommand from the host, all other SMART subcommands – with the exception of SMART Enable Operations – are disabled, and invalid and will be aborted by the device (including the SMART Disable Operations subcommand), returning the error code as specified in Table 174 on the page 232.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or SMART Save Attribute Values command.

10.43.1.10 SMART Return Status (Subcommand Dah)

This command is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device saves any updated Pre-failure type Attribute Values to the reserved sector and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, the device loads 4Fh into the Cylinder Low register, C2h into the Cylinder High register.

If the device detects a Threshold Exceeded Condition, the device loads F4h into the Cylinder Low register, 2Ch into the Cylinder High register.

10.43.1.11 SMART Enable/Disable Automatic Off-Line (Subcommand DBh)

This subcommand enables and disables the optional feature that causes the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's non-volatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled.

A value of zero written by the host into the device's Sector Count Register before issuing this subcommand shall cause the feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to non-volatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F8h written by the host into the device's Sector Count Register before issuing this subcommand shall cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vender specific and will not change the current Automatic Off-Line Data Collection, but the device may respond with the error code specified in Table 174 on the page.232

10.43.2 Device Attributes Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Values subcommand. All multi-byte fields shown in these data structures are in byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

Description	Bytes	Offset	Value
Data Structure Revision Number	2	00h	0010h
1st Device Attribute	12	02h	
…	..		
…	..		
30th Device Attribute	12	15Eh	
Off-line data collection status	1	16Ah	
Self-test execution status	1	16Bh	
Total time in seconds to complete off-line data collection activity	2	16Ch	
Vender specific	1	16Eh	
Off-line data collection capability	1	16Fh	1Bh
SMART capability	2	170h	0003h
SMART device error logging capability	1	172h	01h
Self-test failure check point	1	173h	
Short self-test completion time in minutes	1	174h	
Extended self-test completion time in minutes	1	175h	
Reserved	12	176h	
Vendor specific	125	182h	
Data structure checksum	1	1FFh	
	512		

Table 163 Device Attribute Data Structure

10.43.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

10.43.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Description	Bytes	Offset
Attribute ID Number (01h to FFh)	1	00h
Status Flags	2	01h
Attribute Value (valid values from 01h to FDh)	1	03h
Vender specific	8	04h
Total Bytes	12	

Table 164 Individual Attribute Data Structure

Attribute ID Numbers: Any non-zero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers.

ID	Attribute Name
0	Indicates that this entry in the data structure is not used
1	Raw Read Error Rate
2	Throughput Performance
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count
7	Seek Error Rate
8	Seek Time Performance
9	Power-On Hours Count
10	Spin Retry Count
12	Device Power Cycle Count
192	Power off Retract count
193	Load Cycle count
194	Temperature
196	Reallocation Event Count
197	Current Pending Sector Count
198	Off-Line Scan Uncorrectable Sector Count
199	Ultra DMA CRC Error Count

Status Flag Definitions

Bit	Definition
0	Pre-failure/advisory bit
	0 An Attribute Value less than or equal to its corresponding Attribute Threshold indicates an advisory condition where the usage or age of the device has exceeded its intended design life period.
	1 An Attribute Value less than or equal to its corresponding attribute threshold indicates a pre-Failure condition where imminent loss of data is being predicted.
1	On-Line Collective bit
	0 The Attribute Value is updated only during Off-Line testing
	1 The Attribute Value is updated during On-Line testing or during both On-Line and Off-Line testing.
2-5	Vendor specific
6-15	Reserved (0)

Normalized Values: The device will perform conversion of the raw Attribute Values to transform them into normalized values, which the host can then compare with the Threshold values. A Threshold is the excursion limit for a normalized Attribute Value.

10.43.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates Automatic Off-Line Data Collection Status.

Bit 7	Automatic Off-Line Data Collection Status
0	Automatic Off-Line Data Collection is disabled.
1	Automatic Off-Line Data Collection is enabled.

Bits 0 thru 6 represents a hexadecimal status value reported by the device.

Value	Definition
0	Off-line data collection never started
2	All segments completed without errors.
4	Off-line data collection suspended by interrupting command
5	Off-line data collecting aborted by interrupting command
6	Off-line data collection aborted with fatal error

10.43.2.4 Self-test execution status

Bit **Definition**

0-3 Percent Self-test remaining

An approximation of the percent of the self-test routine remaining until completion in ten percent increments. Valid values are 0 through 9.

4-7 Current Self-test execution status

- **0** The self-test routine completed without error or has never been run
- **1** The self-test routine aborted by the host
- **2** The self-test routine interrupted by the host with a hard or soft reset
- **3** The device was unable to complete the self-test routine due to a fatal error or unknown test error
- **4** The self-test routine completed with unknown element failure
- **5** The self-test routine completed with electrical element failure
- **6** The self-test routine completed with servo element failure
- **7** The self-test routine completed with read element failure
- **15** The self-test routine in progress

10.43.2.5 Total Time in Seconds to Complete Off-line Data Collection Activity

This field tells the host how many seconds the device requires completing the off-line data collection activity.

10.43.2.6 Off-Line Data Collection Capability

Bit **Definition**

0 Execute Off-line Immediate implemented bit

- **0** SMART Execute Off-line Immediate subcommand is not implemented
- **1** SMART Execute Off-line Immediate subcommand is implemented

1 Enable/disable Automatic Off-line implemented bit

- **0** SMART Enable/disable Automatic Off-line subcommand is not implemented
- **1** SMART Enable/disable Automatic Off-line subcommand is implemented

2 abort/restart off-line by host bit

- **0** The device will suspend off-line data collection activity after an interrupting command and resume it after some vendor specific event
- **1** The device will abort off-line data collection activity upon receipt of a new command

3 Off-line Read Scanning implemented bit

- **0** The device does not support Off-line Read Scanning
- **1** The device supports Off-line Read Scanning

4 Self-test implemented bit

- **0** Self-test routine is not implemented
- **1** Self-test routine is implemented

5-7 Reserved (0)

6 Selective self-test implemented bit

- **0** Selective self-test routine is not implemented
- **1** Selective self-test routine is implemented

10.43.2.7 SMART Capability

This word of bit flags describes the SMART capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit	Definition
0	Pre-power mode attribute saving capability If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).
1	Attribute autosave capability If bit = 1, the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.
2-15	Reserved (0)

10.43.2.8 Error Logging Capability

Bit	Definition
7-1	Reserved (0)
0	Error Logging support bit If bit = 1, the device supports the Error Logging

10.43.2.9 Self-test failure check point

This byte indicates the section of self-test where the device detected a failure.

10.43.2.10 Self-test completion time

These bytes are the minimum time in minutes to complete self-test.

10.43.2.11 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

10.43.3 Device Attribute Thresholds Data Structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Thresholds. All multi-byte fields shown in these data structures follow the ATA/ATAPI-7 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Description	Bytes	Offset	Value
Data Structure Revision Number	2	00h	0010h
1st Attribute Threshold	12	02h	
…	..		
…	..		
30th Attribute Threshold	12	15Eh	
Reserved	18	16Ah	00h
Vendor specific	131	17Ch	00h
Data structure checksum	1	1FFh	
	512		

Table 165 Device Attribute Thresholds Data Structure

10.43.3.1 Data Structure Revision Number

This value is the same as the value used in the Device Attributes Values Data Structure.

10.43.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

Description	Bytes	Offset
Attribute ID Number (01h to FFh)	1	00h
Attribute Threshold	1	01h
Reserved (00h)	10	02h
Total Bytes	12	

Table 166 Individual Threshold Data Structure

10.43.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

10.43.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable.

10.43.3.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

10.43.4 SMART Log Directory

0 defines the 512 bytes that make up the SMART Log Directory. The SMART Log Directory is SMART Log Address zero and is defined as one sector long.

Description	Bytes	Offset
SMART Logging Version	2	00h
Number of sectors in the log at log address 1	1	02h
Reserved	1	03h
Number of sectors in the log at log address 2	1	04h
Reserved	1	05h
…	…	…
Number of sectors in the log at log address 255	1	1Feh
Reserved	1	1FFh
	512	

Table 167 SMART Log Directory

The value of the SMART Logging Version word shall be 01h. The logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

10.43.5 SMART summary error log sector

The following defines the 512 bytes that make up the SMART summary error log sector. All multi-byte fields shown in this data structure follow the ATA/ATAPI-7 specifications for byte ordering.

Description	Bytes	Offset
SMART error log version	1	00h
Error log index	1	01h
1st error log data structure	90	02h
2nd error log data structure	90	5Ch
3rd error log data structure	90	B6h
4th error log data structure	90	110h
5th error log data structure	90	16Ah
Device error count	2	1C4h
Reserved	57	1C6h
Data structure checksum	1	1FFh
	512	

Table 168 SMART summary error log sector

10.43.5.1 SMART error log version

This value is set to 01h.

10.43.5.2 Error log index

This points the most recent error log data structure. Only values 1 through 5 are valid.

10.43.5.3 Device error count

This field contains the total number of errors. The value will not roll over.

10.43.5.4 Error log data structure

Data format of each error log structure is shown below.

Description	Bytes	Offset
1st error log data structure	12	00h
2nd error log data structure	12	0Ch
3rd error log data structure	12	18h
4th error log data structure	12	24h
5th error log data structure	12	30h
Error data structure	30	3Ch
	90	

Table 169 Error log data structure

Command data structure: Data format of each command data structure is shown below.

Description	Bytes	Offset
Device Control register	1	00h
Features register	1	01h
Sector count register	1	02h
Sector number register	1	03h
Cylinder Low register	1	04h
Cylinder High register	1	05h
Device/Head register	1	06h
Command register	1	07h
Timestamp (milliseconds from Power On)	4	08h
	12	

Table 170 Command data structure

Error data structure: Data format of error data structure is shown below.

Description	Bytes	Offset
Reserved	1	00h
Error register	1	01h
Sector count register	1	02h
Sector number register	1	03h
Cylinder Low register	1	04h
Cylinder High register	1	05h
Device/Head register	1	06h
Status register	1	07h
Extended error data (vendor specific)	19	08h
State	1	1Bh
Life timestamp (hours)	2	1Ch
	30	

Table 171 Error data structure

State field contains a value indicating the device state when command was issued to the device.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle
x4h	SMART Off-line or Self-test
x5h-xAh	Reserved
xBh-xFh	Vendor specific
	Note: The value of x is vendor specific.

10.43.6 Self-test log data structure

The following defines the 512 bytes that make up the Self-test log sector. All multi-byte fields shown in these data structures follow the ATA/ATAPI-7 specifications for byte ordering.

Description	Bytes	Offset
Data structure revision	2	00h
Self-test number	1	n*18h+02h
Self-test execution status	1	n*18h+03h
Life time power on hours	2	n*18h+04h
Self-test failure check point	1	n*18h+06h
LBA of first failure	4	n*18h+07h
Vendor specific	15	n*18h+0Bh
…		
Vendor specific	2	1Fah
Self-test index	1	1FCh
Reserved	2	1FDh
Data structure checksum	1	1FFh
	512	

Note: n is 0 through 20

Table 172 Self-test log data structure

The data structure contains the descriptor of Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors.

After 21 descriptors have been recorded, the oldest descriptor will be overwritten with new descriptor.

Self-test index points the most recent descriptor. When there is no descriptor the value is 0. When there is descriptor(s) the value is 1 through 21.

10.43.7 Selective self-test log data structure

The Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. The following table defines the contents of the Selective self-test log which is 512 bytes long. All multi-byte fields shown in these data structures follow the ATA/ATAPI-7 specifications for byte ordering.

Description	Bytes	Offset	Read/Write
Data structure revision	2	00h	**R/W**
Starting LBA for test span 1	8	02h	**R/W**
Ending LBA for test span 1	8	0Ah	**R/W**
Starting LBA for test span 2	8	12h	**R/W**
Ending LBA for test span 2	8	1Ah	**R/W**
Starting LBA for test span 3	8	22h	**R/W**
Ending LBA for test span 3	8	2Ah	**R/W**
Starting LBA for test span 4	8	32h	**R/W**
Ending LBA for test span 4	8	3Ah	**R/W**
Starting LBA for test span 5	8	42h	**R/W**
Ending LBA for test span 5	8	4Ah	**R/W**
Reserved	256	52h	**Reserved**
Vendor specific	154	152h	**Vendor specific**
Current LBA under test	8	1Ech	**Read**
Current span under test	2	1F4h	**Read**
Feature flags	2	1F6h	**R/W**
Vendor specific	4	1F8h	**Vendor specific**
Selective self-test pending time	2	1FCh	**R/W**
Reserved	1	1Feh	**Reserved**
Data structure checksum	1	1FFh	**R/W**
	512		

Table 173 Selective self-test log data structure

10.43.7.1 Feature flags

The Feature flags define the features of Selective self-test to be executed.

Bit	Description
0	Vendor specific
1	When set to one, perform off-line scan after selective test.
2	Vendor specific
3	When set to one, off-line scan after selective test is pending.
4	When set to one, off-line scan after selective test is active.
5-15	Reserved.

Table 174 Selective self-test feature flags

10.43.8 Error Reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Error Condition	Status Register	Error Register
A SMART FUNCTION SET command was received by the device without the required key being loaded into the Cylinder High and Cylinder Low registers.	51h	04h
A SMART FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A SMART FUNCTION SET command subcommand other than SMART ENABLE OPERATIONS was received by the device while the device was in a “SMART disabled” state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure.	51h	10h or 40h
The device is unable to write to its Attribute Values data structure.	51h	10h ~~or 01h~~

Table 175 SMART Error Codes

10.44Standby (E2h/96h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 176 Standby Command (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately, and set auto power down timeout parameter (standby timer).

When the Standby mode is entered, the drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The automatic power down sequence is enabled and the timer starts counting down when the drive returns to Idle mode.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, the timeout interval (Standby Timer) is NOT disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is shown blow:

Value	Timeout
0	Timer disabled
1-240	Value * 5 seconds
241-251	(Value-240) * 30 minutes
252	21 minutes
253	8 hours
254	21 minutes 10 seconds
255	21 minutes 15 seconds

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

10.45 Standby Immediate (E0h/94h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 177 Standby Immediate Command (E0h/94h)

The Standby Immediate command causes the device to enter Standby mode immediately.

The device is spun down but the interface remains active. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode, the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect the auto power down timeout parameter.

10.46 Write Buffer (E8h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Table 178 Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

10.47Write DMA (Cah/CBh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below…							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 179 Write DMA Command (Cah/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device, then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 – 27. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 – 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 – 15 (Low), 16 – 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 – 27. (L=1)

10.48Write DMA FUA Ext (3Dh)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	1	1	0	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 180 Write DMA FUA Ext Command (3Dh)

The Write DMA FUA Ext command transfers one or more sectors of data from the host to the device, and then the data is written to the disk media. This command provides the same function as the Write DMA Ext command except that the transferred data shall be written to the media before the ending status for this command is reported also when write caching is enabled.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an unrecoverable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

10.49 Write DMA Ext (35h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	0	1	0	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 181 Write DMA Ext Command (35h)

The Write DMA Ext command transfers one or more sectors of data from the host to the device, and then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

10.50 Write FPDMA Queued (61h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		V	1	-	0	-	-	-	-
Command		0	1	1	0	0	0	0	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 182 Write FPDMA Queued Command (61h)

The Write FPDMA Queued command transfers one or more sectors of data from the host to the device, and then the data is written to the disk media.

If an unrecoverable error occurs, the write will be terminated at the failing sector

Output Parameters To The Device

Feature Current	The number of sectors to be transferred low order, bits (7:0).
Feature Previous	The number of sectors to be transferred high order, bits (15:8).
Sector Count Current	.
TAG (bits 7-3)	The TAG value shall be assigned to be different from all other queued commands. The value shall not exceed the maximum queue depth specified by the Word 75 of the Identify Device information.
Sector Count Previous	
PRIO (bits 7)	The Priority (PRIO) value shall be assigned by the host based on the priority of the command issued. The device shall make a best effort to complete High priority requests in a more timely fashion than Normal priority requests. The Priority values are defined as follows: 0b Normal priority 1b High priority
Sector Number Current	LBA (7:0)
Sector Number Previous	LBA (31:24)
Cylinder Low Current	LBA (15:8)
Cylinder Low Previous	LBA (39:32)
Cylinder High Current	LBA (23:16)
Cylinder High Previous	LBA (47:40)
Device/Head	
FUA (bit 7)	When the FUA bit is set to 1, the completion status is indicated after the transferred data are written to the media also when Write Cache is enabled. When the FUA bit is set to 0, the completion status may be indicated before the transferred data are written to the media successfully when Write Cache is enabled.

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24)of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8)of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32)of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16)of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40)of the address of the first unrecoverable error.

10.51Write Log Ext (3Fh)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Device/Head		1	-	1	D	-	-	-	-
Command		0	0	1	1	1	1	1	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		…See Below…							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder Low	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Cylinder High	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Device/Head		-	-	-	-	-	-	-	-
Status		…See Below…							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 183 Write Log Ext Command (3Fh)

This command writes a specified number of 512 byte data sectors to the specific log. The device shall interrupt for each DRQ block transferred.

Output Parameters To The Device

Sector Count Current	The number of sectors to be written to the specified log low order, bits (7:0).
Sector Count Previous	The number of sectors to be written to the specified log high orders, bits (15:8). If the number of sectors is greater than the number indicated in the Log directory, which is available in Log number zero, the device shall return command aborted. The log transferred to the device shall be stored by the device starting at the first sector in the specified log.
Sector Number Current	The log to be written as described in 0 Log address definition. If the host attempts to write to a read only log address, the device shall return command aborted.
Cylinder Low Current	The first sector of the log to be written low order, bits (7:0).
Cylinder Low Previous	The first sector of the log to be written high order, bits (15:8).

If the feature set associated with the log specified in the Sector Number register is not supported or enabled, or if the values in the Sector Count, Sector Number or Cylinder Low registers are invalid, the device shall return command aborted. If the host attempts to write to a read only log address, the device shall return command aborted.

10.52 Write Multiple (C5h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 184 Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, and then the data is written to the disk media.

Command execution is identical to the Write Sector(s) command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

10.53Write Multiple Ext (39h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	1	0	0	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 185 Write Multiple Ext Command (39h)

The Write Multiple Ext command transfers one or more sectors from the host to the device, and then the data is written to the disk media.

Command execution is identical to the Write Sector(s) Ext command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors shall be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

10.54Write Multiple FUA Ext (CEh)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		1	1	0	0	1	1	1	0

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 186 Write Multiple FUA Ext Command (CEh)

The Write Multiple Ext command transfers one or more sectors from the host to the device, and then the data is written to the disk media. This command provides the same function as the Write Multiple Ext command except that the transferred data shall be written to the media before the ending status for this command is reported also when write caching is enabled.

Command execution is identical to the Write Sector(s) Ext command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors shall be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

10.55 Write Sector(s) (30h/31h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 187 Write Sector(s) Command (30h/31h)

The Write Sector(s) command transfers one or more sectors from the host to the device,and then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)
R	The retry bit, but this bit is ignored.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

10.56 Write Sector(s) Ext (34h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	-	-	-	-	-	-	-	-
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	0	1	1	0	1	0	0

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 188 Write Sector(s) Ext Command (34h)

The Write Sector(s) Ext command transfers one or more sectors from the host to the device, and then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order bits (15:8). If zero is specified, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

10.57Write Stream DMA (3Ah)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	-	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	1	1	0	1	0

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	CCTO
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	SE	DWE	DRQ	COR	IDX	ERR
0	V	V	0	-	0	-	V

Table 189 Write Stream DMA Command (3Ah)

The Write Stream DMA command allows the host to write data using the DMA data transfer protocol. This command allows for the host to specify to the device that additional actions need to be performed prior to the completion of the command if the required bits are set.

If the Write Continuous bit is set to one, the device shall not stop execution of the command due to errors. If the WC bit is set to one and errors occur in the transfer or writing of the data, the device shall continue to transfer the amount of data requested and then provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, ICRC, IDNF, or ABRT, reported in the error log. If the WC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one, In all cases, the device shall attempt to transfer the amount of data requested within the Command Completion Time Limit event if some data transferred is in error.

Output Parameters To The Device

Feature Current

URG (bit7)	URG specifies an urgent transfer request. The Urgent bit specifies that the command should be completed in the minimum possible time by the device and shall be completed within the specified Command Completion Time Limit.
WC (bit6)	WC specifies Write Continuous mode enabled. If the Write Continuous bit is set to one, the device shall not stop execution of the command due to errors. If the WC bit is set to one and errors occur in transfer or writing of the data, the device shall continue to transfer the amount of data requested and then provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, ICRC, IDNF or ABRT reported in the error log. If the WC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one. In all cases, the device shall attempt to transfer the amount of data requested within the Command Completion Time Limit even if some data transferred is in error.
F (bit5)	F specifies that all data for the specified stream shall be flushed to the media before command complete is reported when set to one.
HSE (bit4)	HSE (Handle Stream Error) specifies that this command starts at the LBA of the last reported error for this stream, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier.
Stream ID (bit 0..2)	Stream ID specifies the stream being written. The device shall operate according to the Stream ID set by the Write Stream command.
Feature Previous CCTL (7:0)	The time allowed for the current command's completion is calculated as follows: Command Completion Time Limit = (content of the Feature register Previous) * (Identify Device words (99:98)) useconds If the value is zero, the device shall use the Default CCTL supplied with a previous Configure Stream command for this Stream ID. If the Default CCTL is zero, or no previous Configure Stream command was defined for this Stream ID, the device will ignore the CCTL. The time is measured from the write of the command register to the final INTRQ for command completion. The minimum CCTL is 50ms.CCTL is set to 50ms when the specified value is shorter than 50ms.
Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.
CCTO (Error, bit 0)	CCTO bit shall be set to one if a Command Completion Time Limit Out error has occurred.

10.58 Write Stream PIO (3Bh)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	-	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		1	1	1	D	-	-	-	-
Command		0	0	1	1	1	0	1	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	CCTO
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	SE	DWE	DRQ	COR	IDX	ERR
0	V	V	0	-	0	-	V

Table 190 Write Stream PIO Command (3Bh)

This command writes from 1 to 65536 sectors as specified in the Sector Count register. A sector count of 0 requests 65536 sectors.

If the Write Continuous bit is set to one, the device shall not stop execution of the command due to errors. If the WC bit is set to one and errors occur in the transfer or writing of the data, the device shall continue to transfer the amount of data requested and then provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, IDNF, or ABRT, reported in the error log. If the WC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one, In all cases, the device shall attempt to transfer the amount of data requested within the Command Completion Time Limit event if some data transferred is in error.

Output Parameters To The Device

Feature Current

URG (bit7)	URG specifies an urgent transfer request. The Urgent bit specifies that the command should be completed in the minimum possible time by the device and shall be completed within the specified Command Completion Time Limit.
WC (bit6)	WC specifies Write Continuous mode enabled. If the Write Continuous bit is set to one, the device shall not stop execution of the command due to errors. If the WC bit is set to one and errors occur in transfer or writing of the data, the device shall continue to transfer the amount of data requested and then provide ending status with BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, IDNF or ABRT reported in the error log. If the WC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one. In all cases, the device shall attempt to transfer the amount of data requested within the Command Completion Time Limit even if some data transferred is in error.
F (bit5)	F specifies that all data for the specified stream shall be flushed to the media before command complete is reported when set to one.
HSE (bit4)	HSE (Handle Stream Error) specifies that this command starts at the LBA of the last reported error for this stream, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier.
Stream ID (bit 0..2)	Stream ID specifies the stream being written. The device shall operate according to the Stream ID set by the Write Stream command.
Feature Previous	The time allowed for the current command's completion is calculated as follows: Command Completion Time Limit = (content of the Feature register Previous) * (Identify Device words (99:98)) useconds If the value is zero, the device shall use the Default CCTL supplied with a previous Configure Stream command for this Stream ID. If the Default CCTL is zero, or no previous Configure Stream command was defined for this Stream ID, the device will ignore the CCTL. The time is measured from the write of the command register to the final INTRQ for command completion. The minimum CCTL is 50ms.CCTL is set to 50ms when the specified value is shorter than 50ms.
Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.
CCTO (Error, bit 0)	CCTO bit shall be set to one if a Command Completion Time Limit Out error has occurred.

10.59 Write Uncorrectable Ext (45h)

Command Block Output Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Feature	Current	V	V	V	V	V	V	V	V
	Previous	-	-	-	-	-	-	-	-
Sector Count	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Sector Number	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder Low	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Cylinder High	Current	V	V	V	V	V	V	V	V
	Previous	V	V	V	V	V	V	V	V
Device/Head		-	1	-	D	-	-	-	-
Command		0	1	0	0	0	1	0	1

Command Block Input Registers									
Register		7	6	5	4	3	2	1	0
Data Low		-	-	-	-	-	-	-	-
Data High		-	-	-	-	-	-	-	-
Error		...See Below...							
Sector Count	HOB=0	-	-	-	-	-	-	-	-
	HOB=1	-	-	-	-	-	-	-	-
Sector Number	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder Low	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Cylinder High	HOB=0	V	V	V	V	V	V	V	V
	HOB=1	V	V	V	V	V	V	V	V
Device/Head		-	-	-	-	-	-	-	-
Status		...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Table 191 Write Uncorrectable Ext Command (45h)

The Write Uncorrectable Ext command is used to cause the device to report an uncorrectable error when the target sector is subsequently read.

When the Feature field contains a value of 5xh the Write Uncorrectable Ext command shall cause the device to indicate a failure when reads to any of the sectors that are contained in physical block of specified sector are performed. These sectors are referred to as ‘pseudo uncorrectable’ sectors. In this case whenever a pseudo uncorrectable sector is accessed via a read command the drive shall perform normal error recovery to the fullest extent and then set the UNC and ERR bits to indicate the sector is bad.

When the Feature field(7:0) contains a value of Axh the Write uncorrectable ext command shall cause the device to flag the specified sector as ‘flagged uncorrectable’. Flagging a logical sector as uncorrectable shall cause the device to indicate a failure when reads to the specified sector are performed. These sectors are referred to as ‘flagged uncorrectable’ sectors. In this case whenever a ‘flagged uncorrectable’ sector is accessed via a read command the device shall set the UNC and ERR bits to indicate the sector is bad.

If this command is sent to the device with the content of the Features field(7:0) set to anything other than what is defined above the device shall abort the command.

Commands that return UNC and ERR when a pseudo uncorrectable or flagged uncorrectable sector is read include: READ DMA,READ DMA EXT, READ MULTIPLE, READ MULTIPLE EXT, READ SECTOR(S), READ SECTOR(S) EXT, READ VERIFY SECTOR(S), READ, VERIFY SECTOR(S) EXT, READ STREAM EXT, READ STREAM DMA EXT. if the host writes to a ‘pseudo uncorrectable’ or ‘flagged uncorrectable’ sector, the drive shall attempt to write the data to the sector. The write shall clear the uncorrectable status of the sector and make the sector good if possible and the device shall verify that the sector may now be read without error. It is possible that an ‘uncorrectable’ sector location has actual physical errors. In this case read commands and/or write commands shall return ERR status information that is consistent with the error.

If the LOG feature is set to x5h sectors that have been made pseudo uncorrectable when read back shall be listed as failed in the standard error logs and shall cause SMART utilities to indicate failure if too many sectors are uncorrectable. The LOG feature set to xAh shall indicate that reading of pseudo uncorrectable sectors shall not be logged as an error in any standardized error logs.

The pseudo uncorrectable or flagged uncorrectable status of a sector shall remain through a power cycle. If the drive is unable to process a Write Uncorrectable EXT command for any reason the device shall abort the

command.

Output Parameters To The Device

Feature Current	Uncorrectable options 55h :Create a pseudo-uncorrectable error with logging 5Ah :Create a pseudo-uncorrectable error without logging A5h :Created a flagged error with logging AAh :Created a flagged error without logging Other value : Reserved
Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0).
Sector Count Previous	The number of continuous sectors to be transferred high order bits (15:8). If zero is specified, then 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0).
Sector Number Previous	LBA (31:24).
Cylinder Low Current	LBA (15:8).
Cylinder Low Previous	LBA (39:32).
Cylinder High Current	LBA (23:16).
Cylinder High Previous	LBA (47:40).

Input Parameters From The Device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

11.0 Timings

The timing of BSY and DRQ in Status Register are shown in Table 191.

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Power On and COMRESET	Device Busy after Power On	Power On	The device sets BSY(=0) and RDY(=1) to the Status Register and sends a Register FIS to the host.	31 sec
Software Reset	Device Busy after Software Reset	The host asserts SRST(=1) in the Device Control Register and sends a Register FIS to the Device.	The Host sets BSY(=1) to the Status Register.	400 ns
	Device Ready after Software Reset	The host asserts SRST(=1) to the Device Control Register and sends a Register FIS to the Device. Then the host negates SRST(=0) to the Device Control Register and sends a Register FIS to the Device.	The device sets BSY(=0) and RDY(=1) to the Status Register and requests to send a Register FIS to the host.	31 sec
COMRESET	Device Ready after COMRESET	COMRESET Signal asserted	The device sets BSY(=0) and RDY(=1) to the Status Register and sends a Register FIS to the Host.	31 sec
Non-Data command	Device Busy after a Register FIS to issue a command	The host sets proper values in the registers and sends a Register FIS	The host sets BSY(=1) to the Status register	400 ns
	A Register FIS to report Command Complete	The host sets BSY(=1) to the Status Register	The device sets the status of the command to the Status Register and sends a Register FIS to the host	30 sec
PIO Data In command	Device Busy after a Register FIS to issue a command	The host sets proper values in the registers and sends a Register FIS	The host sets BSY(=1) to the Status Register	400 ns
	PIO SETUP FIS for data-in transfer	The host sets BSY(=1) to the Status Register	The device sets BSY(=0) and DRQ(=1) to the Status Register and sends a PIO SETUP FIS to the host.	30 sec
	Device Busy after data-in transfer	A PIO SETUP FIS is transferred to the host.	The host sets BSY(=1) to the Status Register	400 ns
PIO Data Out Command	Device Busy after a Register FIS to issue a command	The host sets proper values in the registers and sends a Register FIS	The host sets BSY(=1) to the Status Register	400 ns
	Device Busy after data-out transfer	The host sends a Data FIS to the device.	The host sets BSY(=1) to the Status Register	400 ns
	PIO SETUP FIS for data-out transfer	The host sets BSY(=1) to the Status Register	The device sets BSY(=0) and DRQ(=1) to the Status Register and sends a PIO SETUP FIS to the host.	30 sec
DMA Data Transfer Command	Device Busy after a Register FIS to issue a command	The hosts sets proper values in the registers and sends a Register FIS	The host sets BSY(=1) to the Status Register.	400 ns

Table 192 Timeout Values

Command category is referred to “10.0 Command DescriptionsCommand Protocol” on page 115.
The abbreviations "ns", "us", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.

We recommend that the host system executes Soft reset and then retries to issue the command if the host system timeout would occur for the device.

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